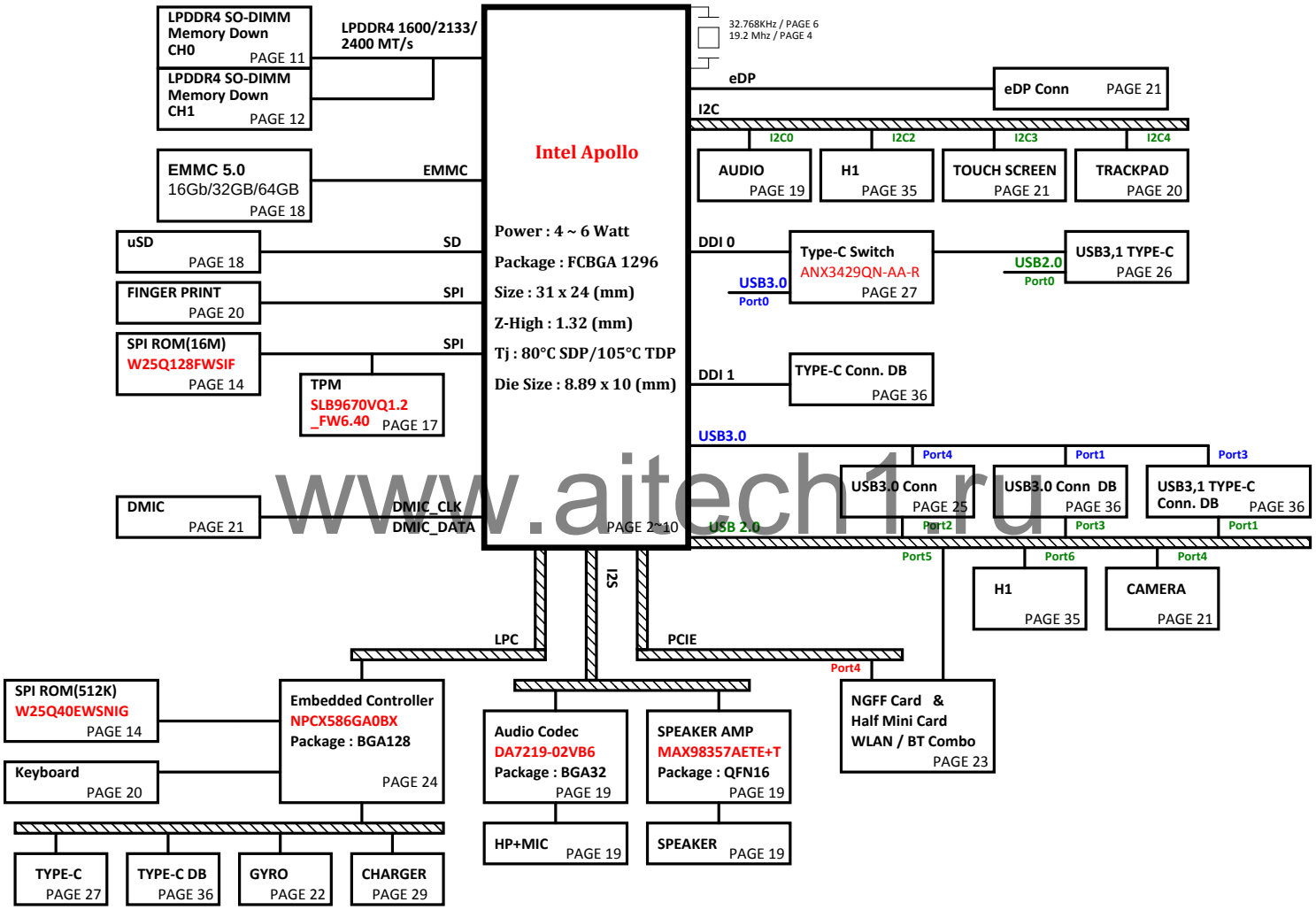
Intel Apollo Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6: BOT



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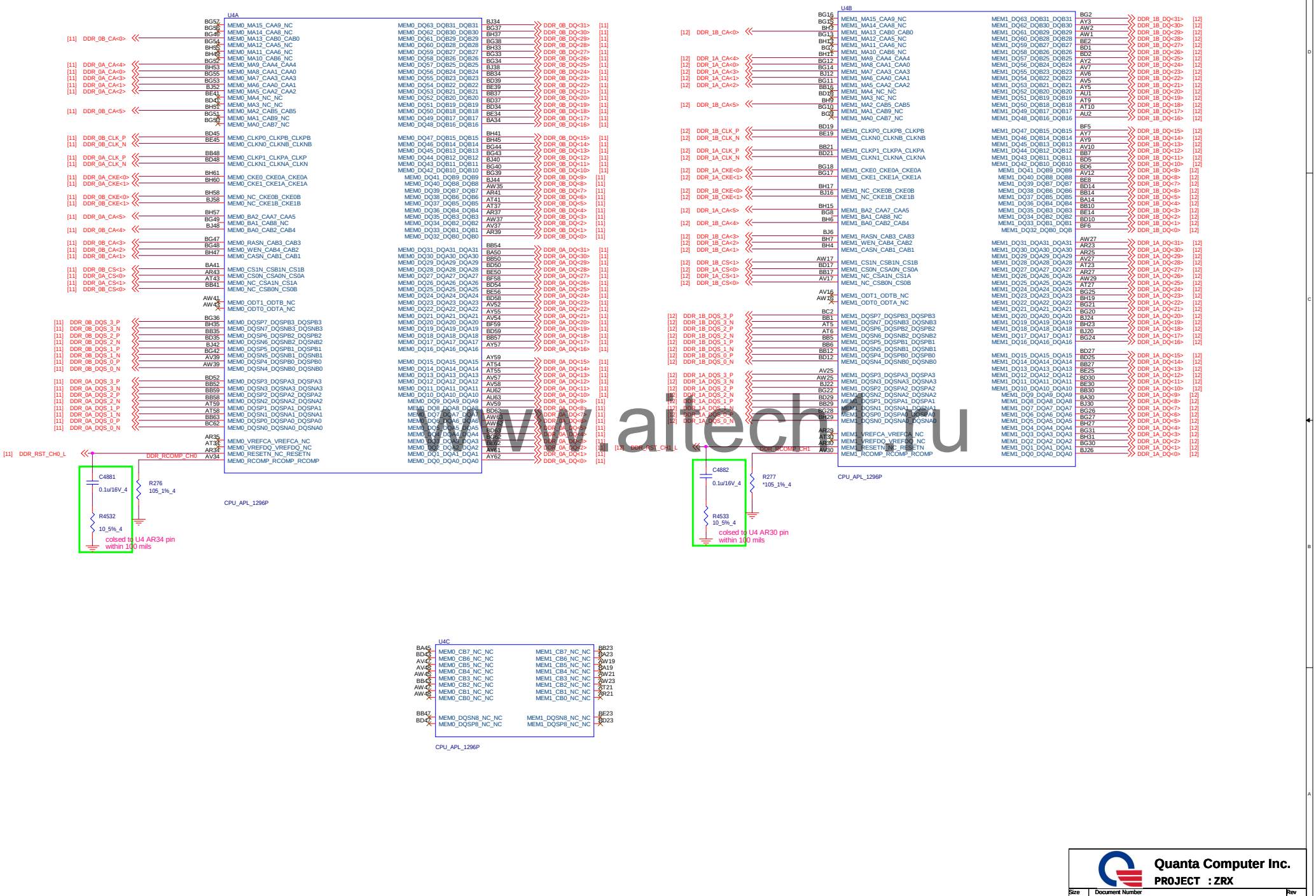
Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Friday, July 21, 2017 Sheet 1 of 38



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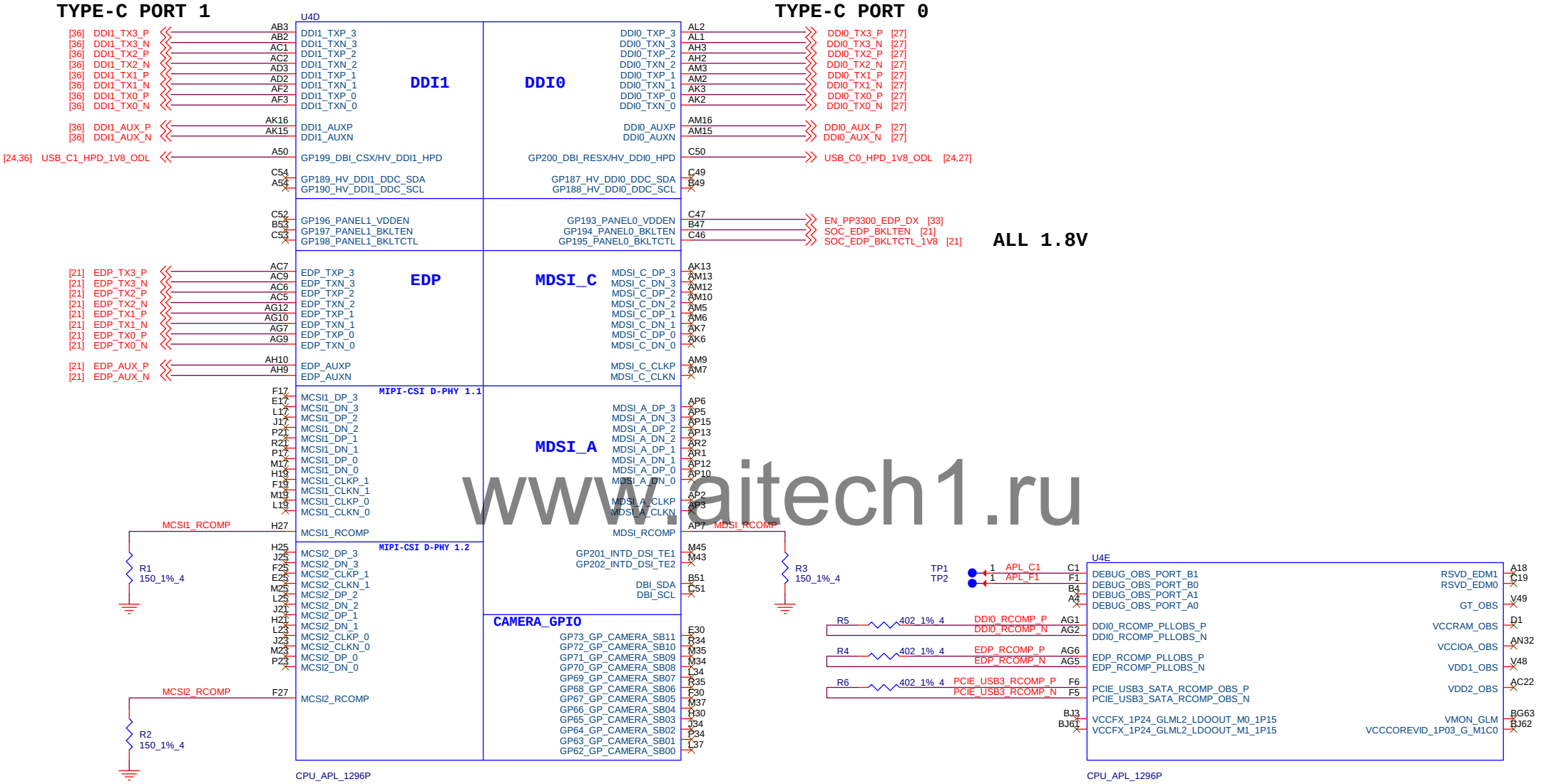
Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: APL MEMORY	Rev: 1A
Date: Friday, July 21, 2017	Sheet 2 of 38	



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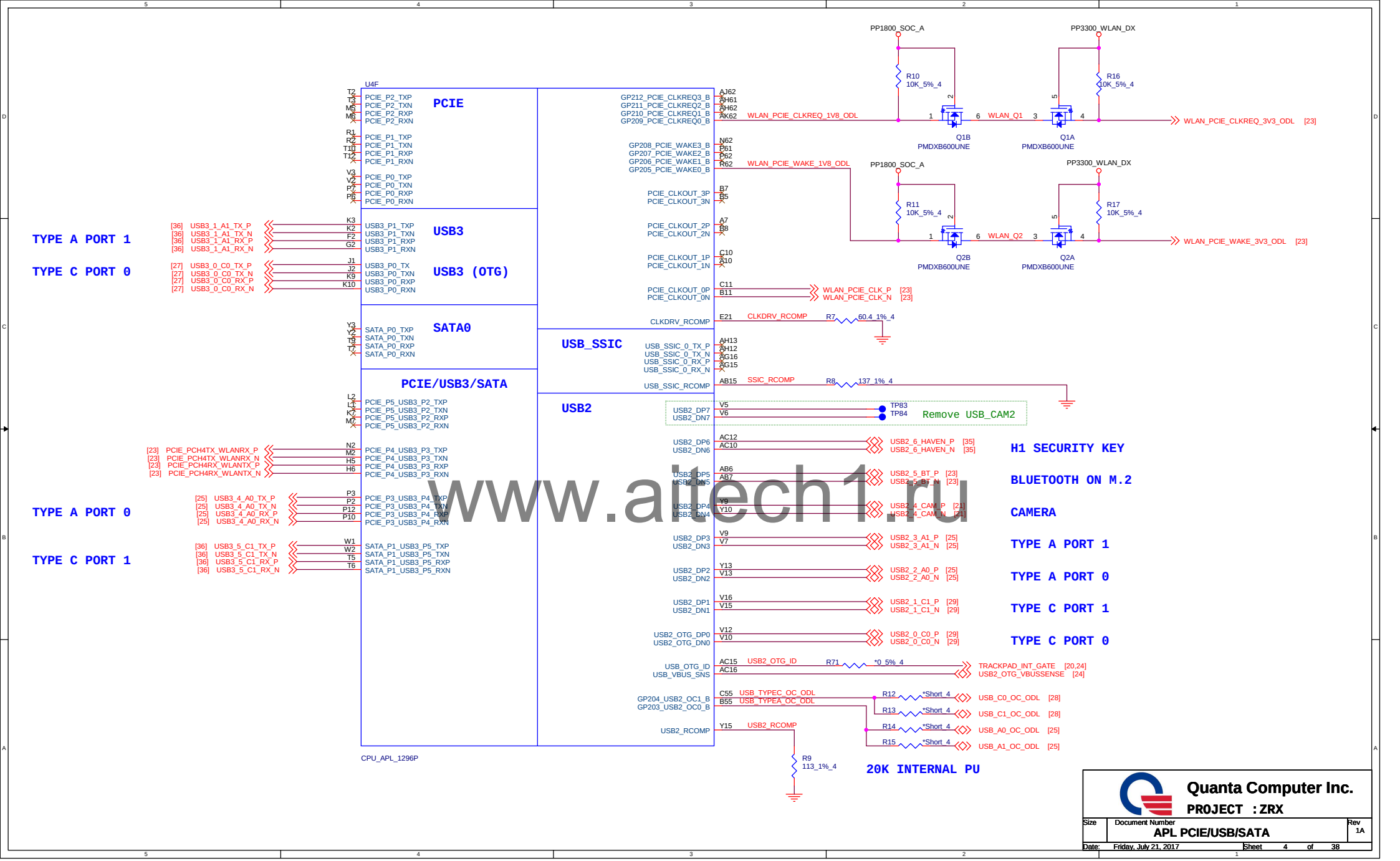
Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	APL eDP/RCOMP	1A

Date: Friday, July 21, 2017 Sheet 3 of 38



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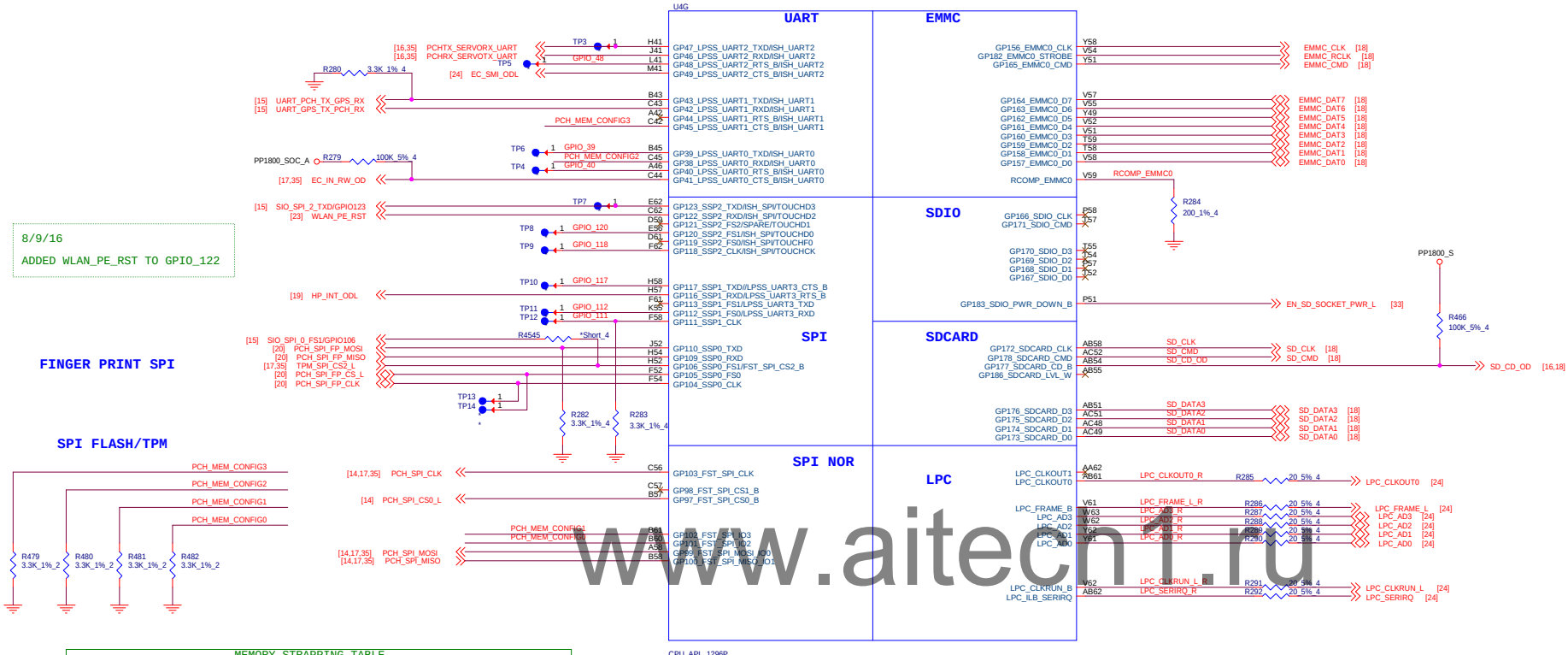
Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	APL PCIE/USB/SATA	1A
Date: Friday, July 21, 2017	Sheet 4 of 38	



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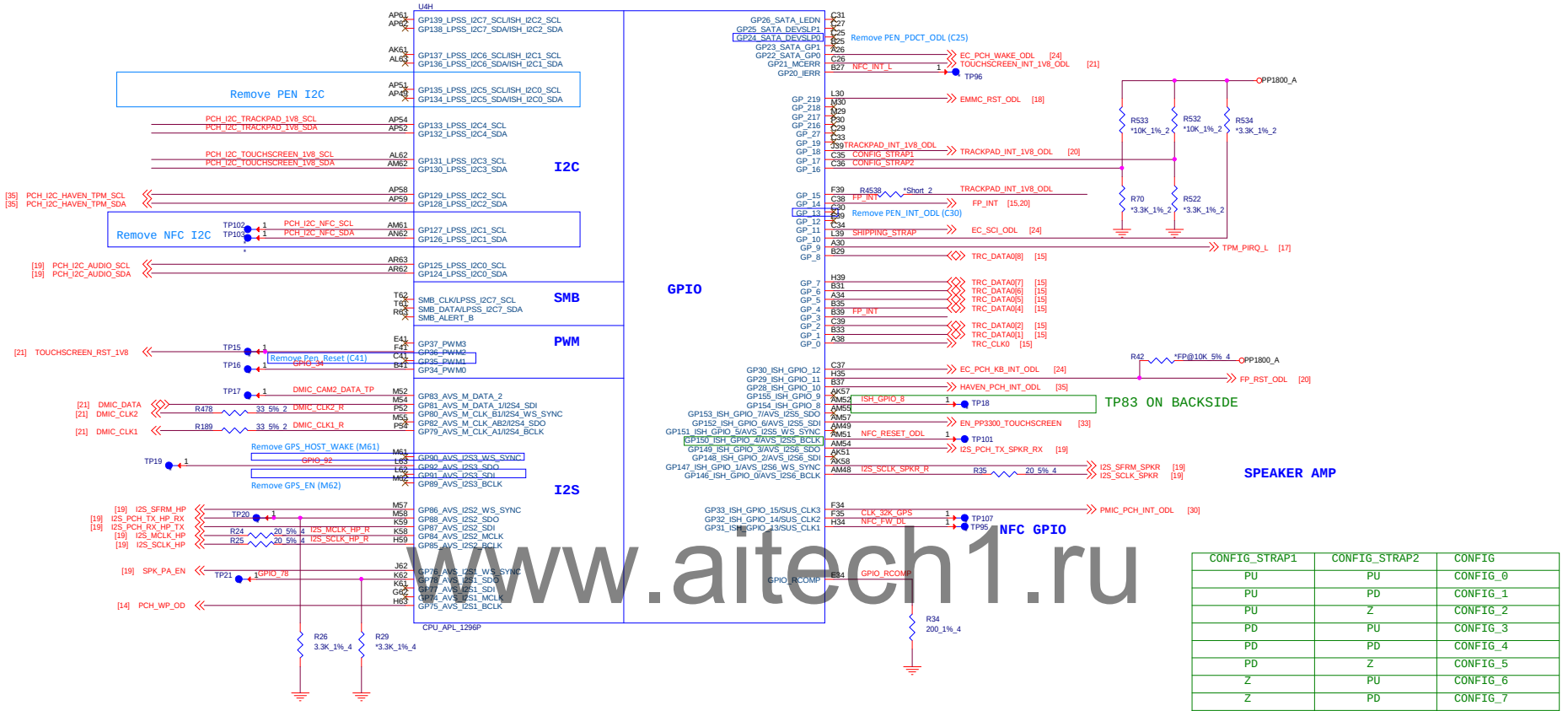
MEMORY STRAPPING TABLE					
Q PN	CONFIG PIN	3	2	1	0
AKD5QZST507	SAMSUNG 8GB K4F8E304HB-MGCJ LF+HF	0	0	0	0
AKD5RZST515	SAMSUNG 4GB K4F6E304HB-MGCJ LF+HF	0	0	0	1
AKD5FWSTL04	MICRON 8GB MT53B512M32D2NP-062WT:C	0	0	1	0
AKD5JWSTL04	MICRON 4GB MT53B256M32D1NP-062 WT:C	0	0	1	1
AKD5RG0TW09	HYNIX 8GB H9HCNNNBPUMLHR-NME	0	1	0	0
AKD5RG0TW08	HYNIX 4GB H9HCNNN8KUMLHR-NME	0	1	0	1
		1	1	1	1

HARDWARE STRAPS (* = SYSTEM STRAP SELECTION)				
GPIO_39: INTERNAL 20K PD *DISABLE CSE ROM BYPASS: 0 ENABLE CSE ROM BYPASS: 1	GPIO_47: INTERNAL 20K PD *DON'T FORCE DNX FW LOAD: 0 FORCE DNX FW LOAD: 1	GPIO_106: INTERNAL 20K PU *MUST BE HIGH WHEN RSM_RST_N DEASSERTS	GPIO_117: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_120: INTERNAL 20K PD *TOP SWAP OVERRIDE DISABLE: 0 TOP SWAP OVERRIDE ENABLE: 1
GPIO_40: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_48: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_111: INTERNAL 20K PU DO NOT BOOT FROM SPI: 1 *BOOT FROM SPI: 0	GPIO_123: INTERNAL 20K PU MUST BE HIGH WHEN RSM_RST_N DEASSERTS	GPIO_121: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS
GPIO_43: INTERNAL 20K PU ENABLE BOOT FROM EMMC: 1 *DISABLE BOOT FROM EMMC: 0	GPIO_104: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_118: INTERNAL 20K PD *NO FLASH DESCRIPTOR OVERRIDE: 0 OVERRIDE FLASH DESCRIPTOR: 1	GPIO_112: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	
GPIO_44: INTERNAL 20K PU *ENABLE BOOT FROM SPI: 1 DISABLE BOOT FROM SPI: 0	GPIO_105: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_110: INTERNAL 20K PU LPC BUFFERS AT 1.8V: 1 *LPC BUFFERS AT 3.3V: 0	GPIO_113: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	

Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	APL UART/SPI/EMMC/SD/LPC	1A

Date: Friday, July 21, 2017 Sheet 5 of 38



CONFIG_STRAP1	CONFIG_STRAP2	CONFIG
PU	PU	CONFIG_0
PU	PD	CONFIG_1
PU	Z	CONFIG_2
PD	PU	CONFIG_3
PD	PD	CONFIG_4
PD	Z	CONFIG_5
Z	PU	CONFIG_6
Z	PD	CONFIG_7
*Z	*Z	CONFIG_8

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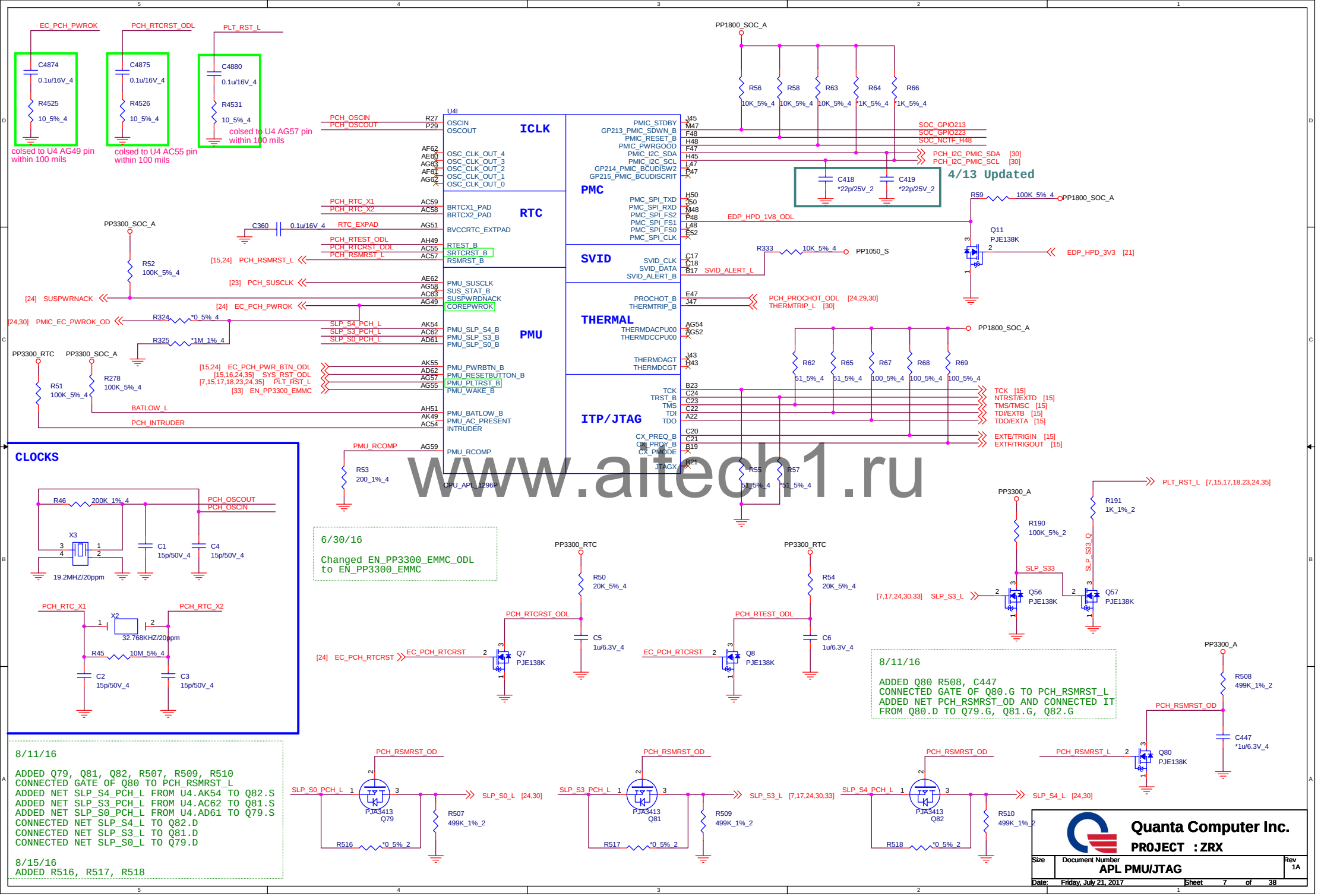
Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	APL I2C/I2S/GPIO	1A

Date: Friday, July 21, 2017 Sheet 6 of 38



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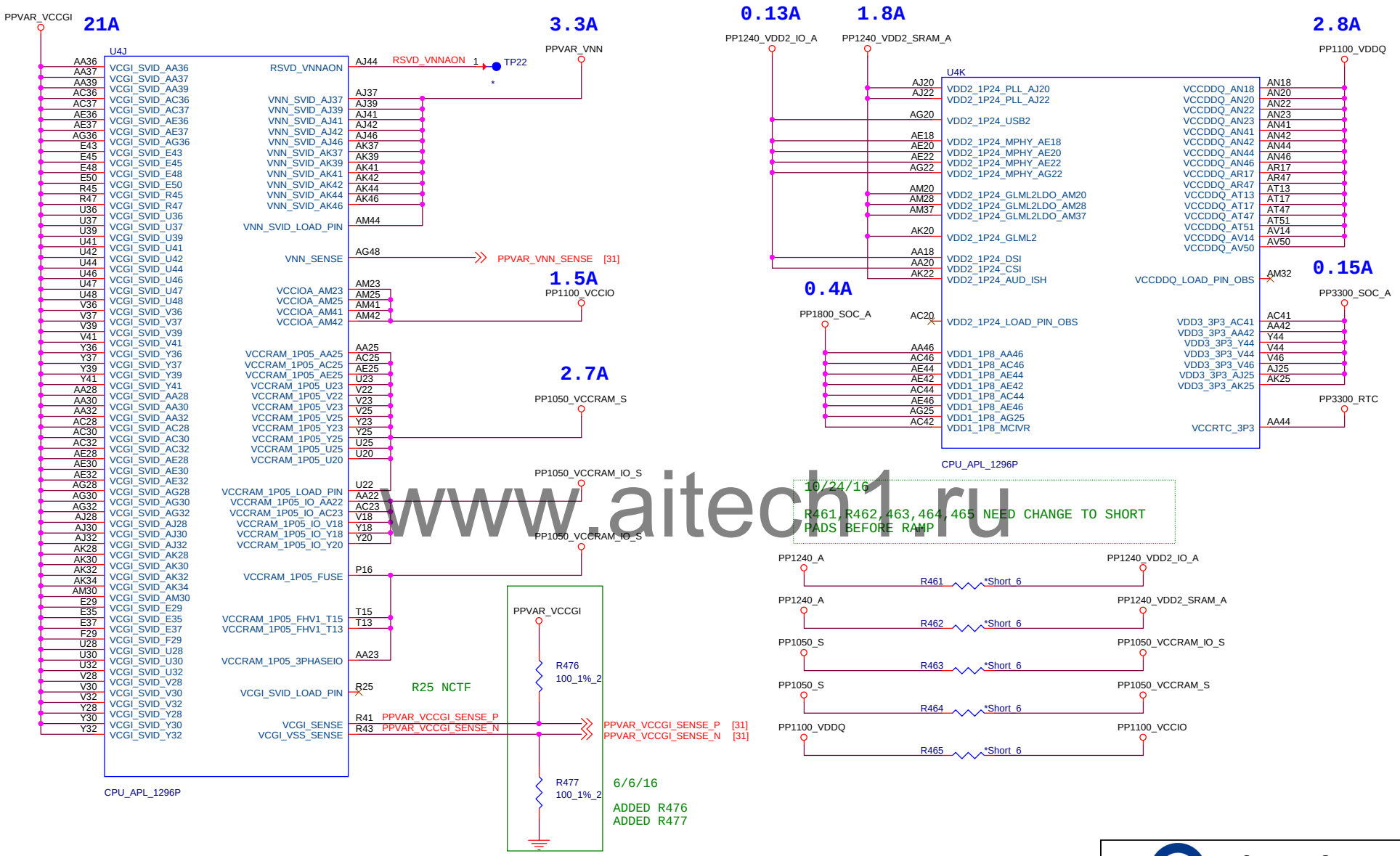

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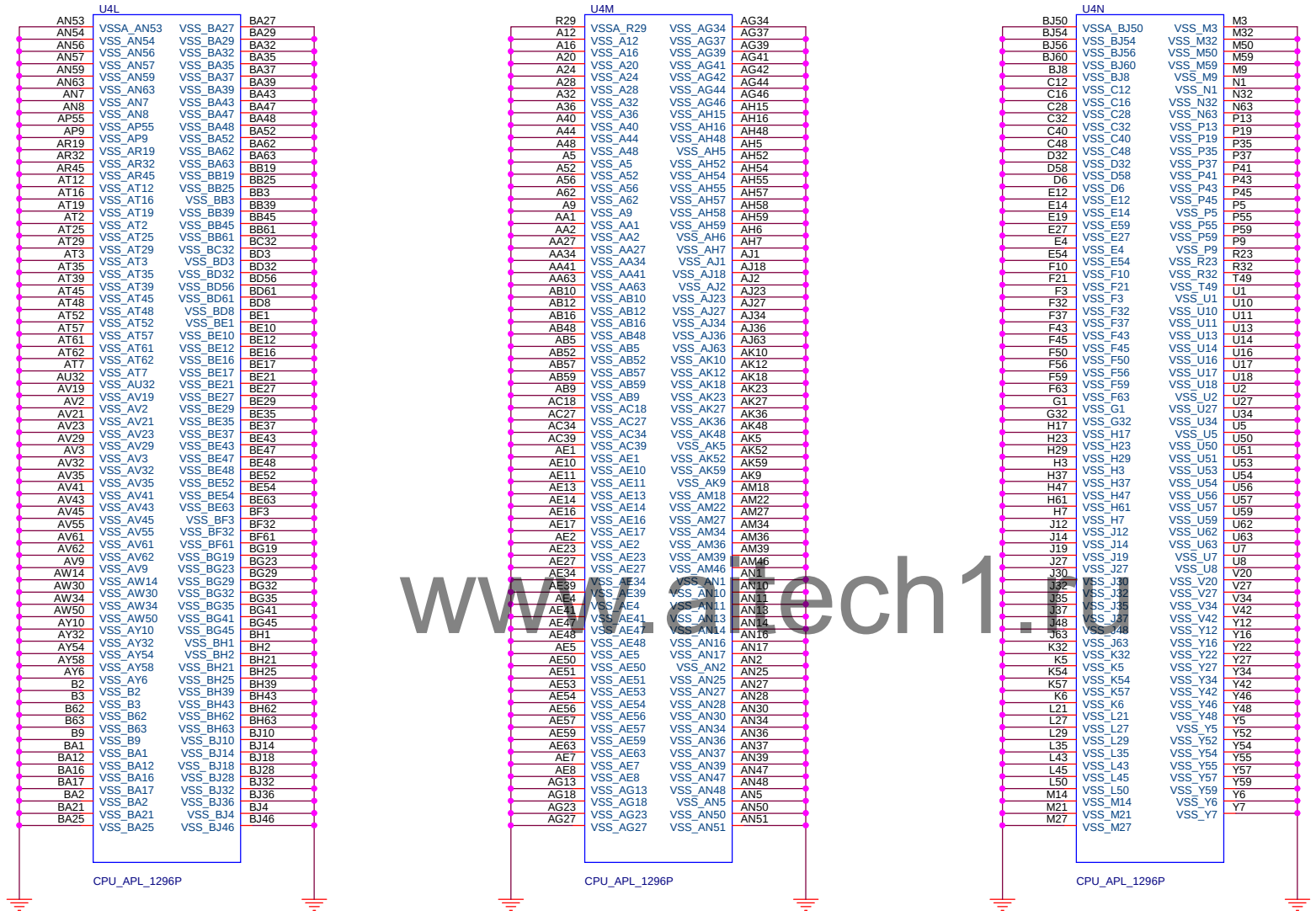
Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: APL POWER	Rev: 1A
Date: Friday, July 21, 2017	Sheet 8 of 38	



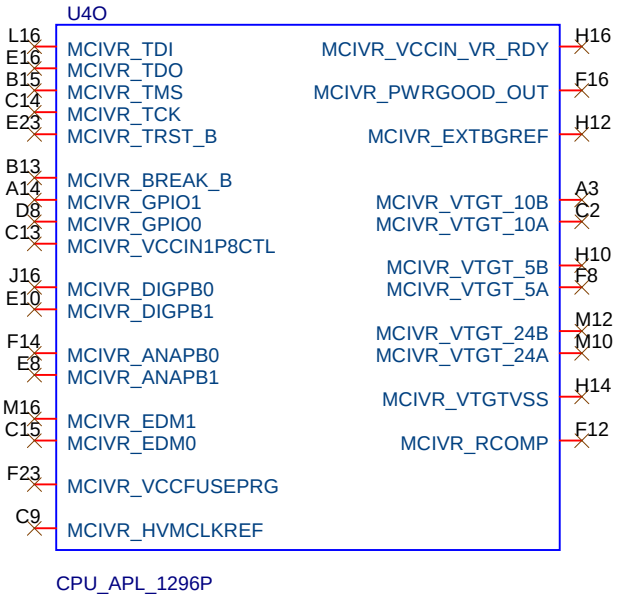
www.elitech1.ir

Quanta Computer Inc.

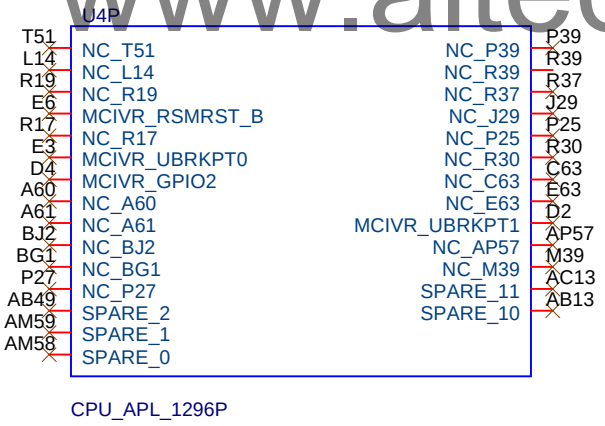
PROJECT : ZRX

Size	Document Number	Rev
	APL GROUND	1A

Date: Friday, July 21, 2017 Sheet 9 of 38



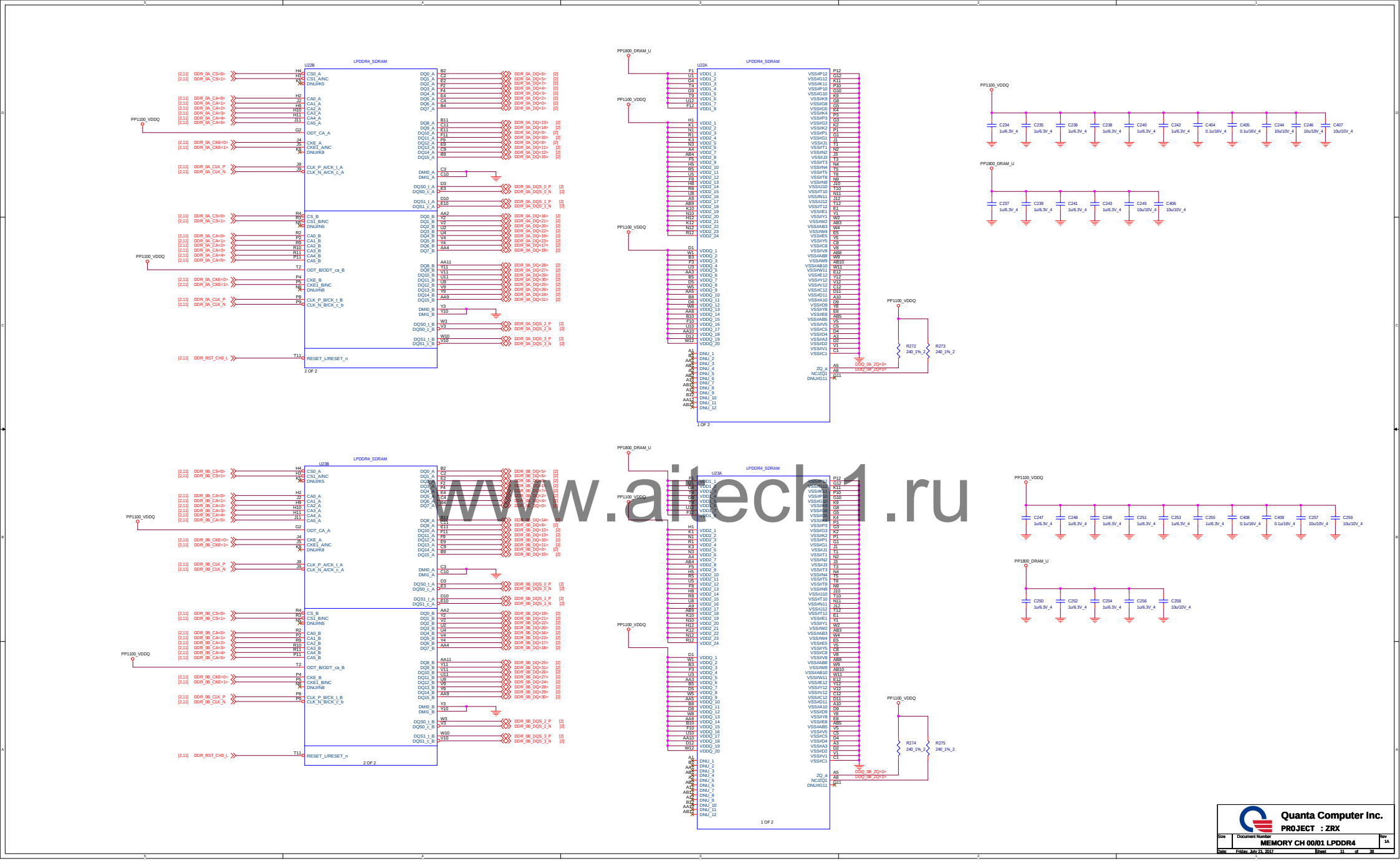
www.aitech1.ru



Quanta Computer Inc.

PROJECT : ZRX

Size	Document Number	Rev
	APL NO CONNECT	1A
Date: Friday, July 21, 2017	Sheet 10 of 38	



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Quanta Computer Inc.
PROJECT : ZRX
Size
Document Number
MEMORY CH 00/01 LPDDR4
Rev 1A
Date: Friday, July 21, 2017
Sheet 11 of 38

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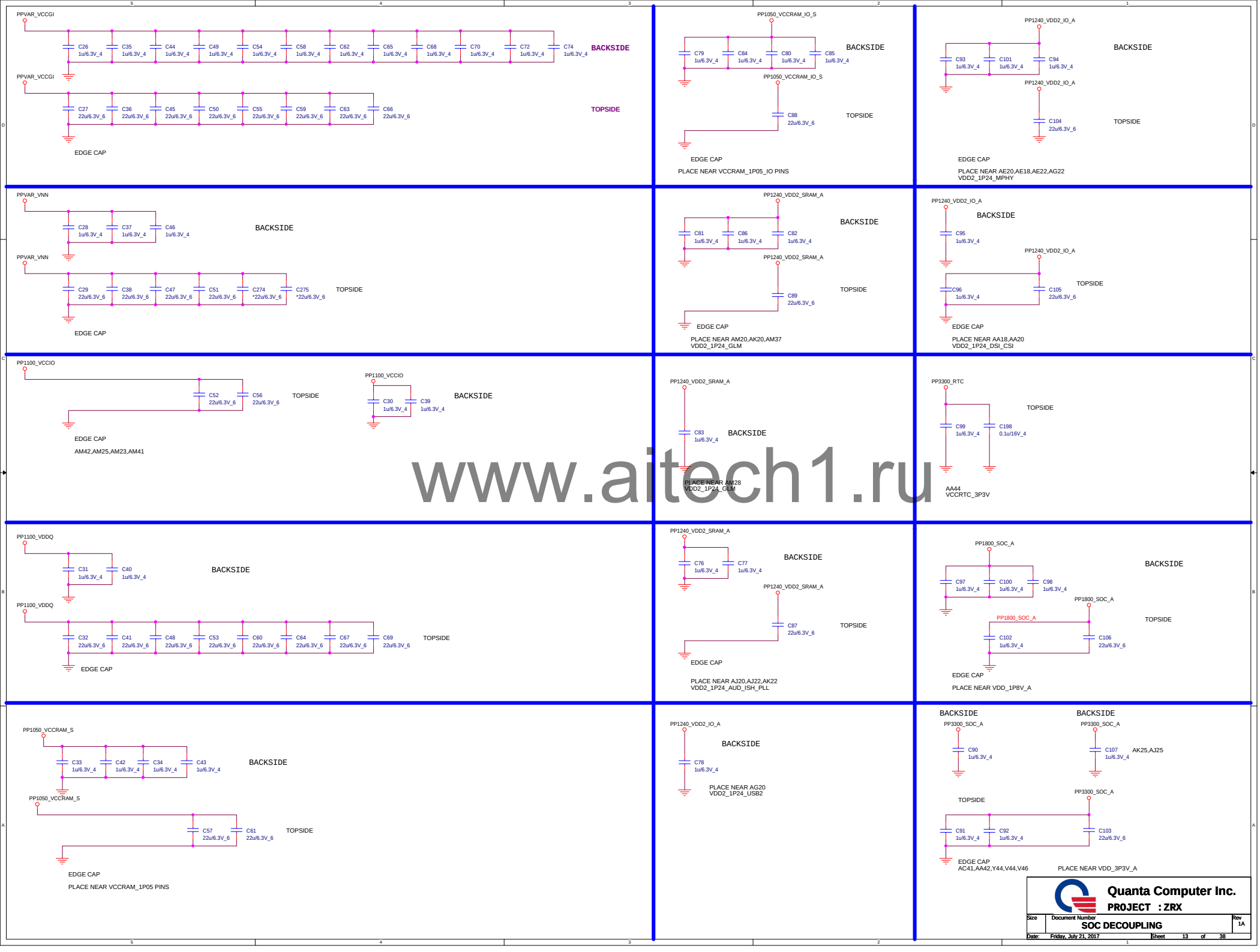
Quanta Computer Inc.
PROJECT : ZRX
Size | Document Number: MEMORY CH 10/11 LPDDR4 | Rev: 1A
Date: Friday, July 21, 2017 | Sheet 12 of 38



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PCH SPI FLASH

8/31/16

ADDED D40, R520
ADDED HAVEN_AP_FLASH_SEL_33A_ODL

PDG IS NOT CLEAR IF CS0 NEEDS PULL-UP
33 OHMS ON SPI SIDE BASED ON PDG

WINBOND: W25Q128FWPIF
GIGADEVICES: 25LQ128CWIG
16MB PCH FLASH
STANDBY CURRENT: 50 UA
MAX CURRENT: 25MA

8/11/16

CHANGED R471 PULLUP TO PP3300_EC
CHANGED U5 TO W25Q128FWPIF

74LVC1G07
1.65-5.5V

KEEP NEAR H1(U95) TO MINIMIZE SPI STUBS

EC SPI FLASH

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DSW STANDBY CURRENT: 10-50 UA
DSW POWERDOWN CURRENT: 1-5 UA

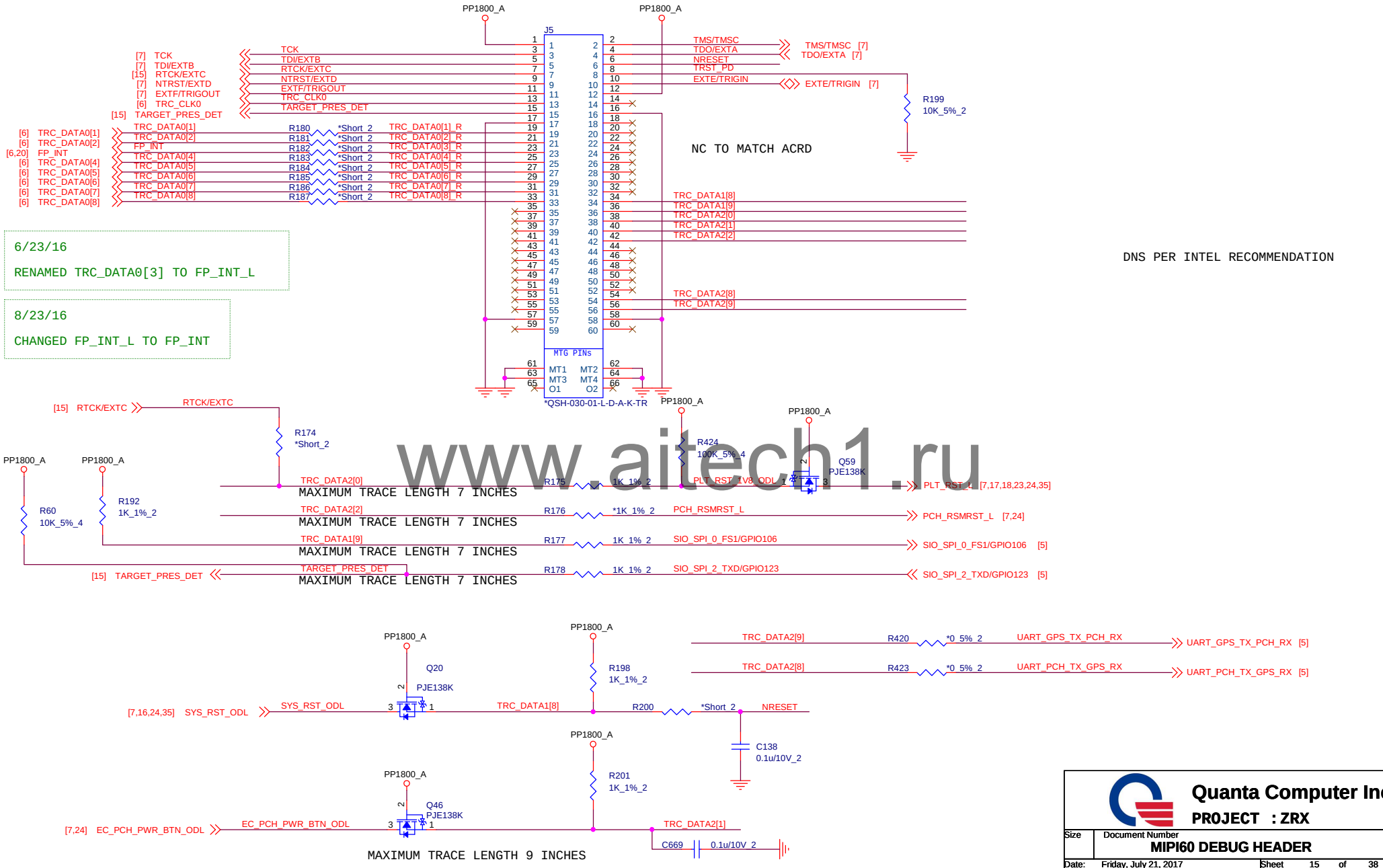
DO WE WANT DO USE THE 1.8V LDO?
ADD 1.8V SPI PART

512KB EC FLASH
MAX CURRENT: 15MA

8/11/16

REMOVED R89, MT1
(Hole1 change to normal hole)

Quanta Computer Inc. PROJECT : ZRX			
Size	Document Number		Rev
	SPI ROM		1A
Date: Friday, July 21, 2017		Sheet 14 of 38	



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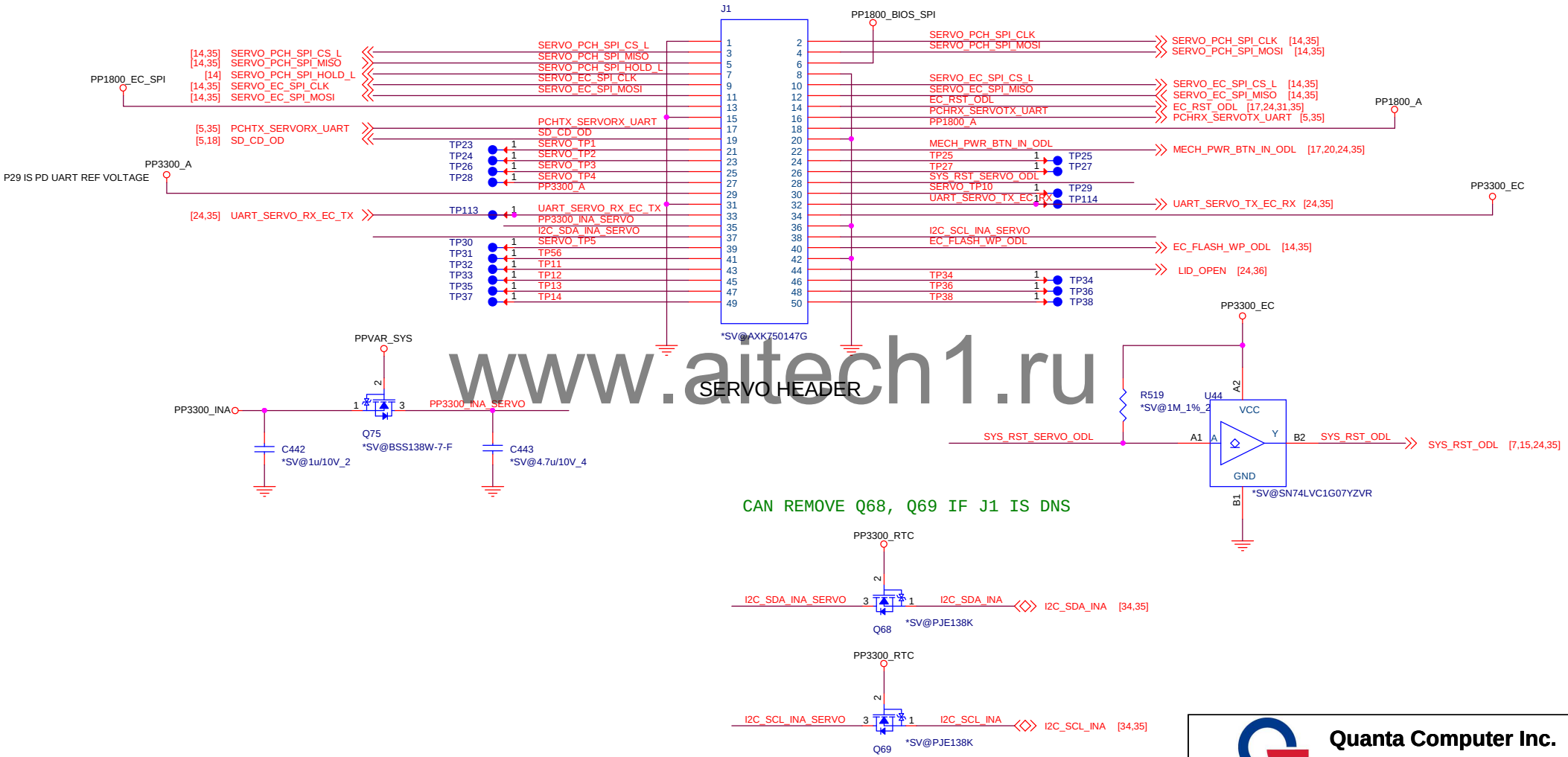
Quanta Computer Inc.

PROJECT : ZRX

Size	Document Number	Rev
	MIPI60 DEBUG HEADER	1A

Date: Friday, July 21, 2017 Sheet 15 of 38



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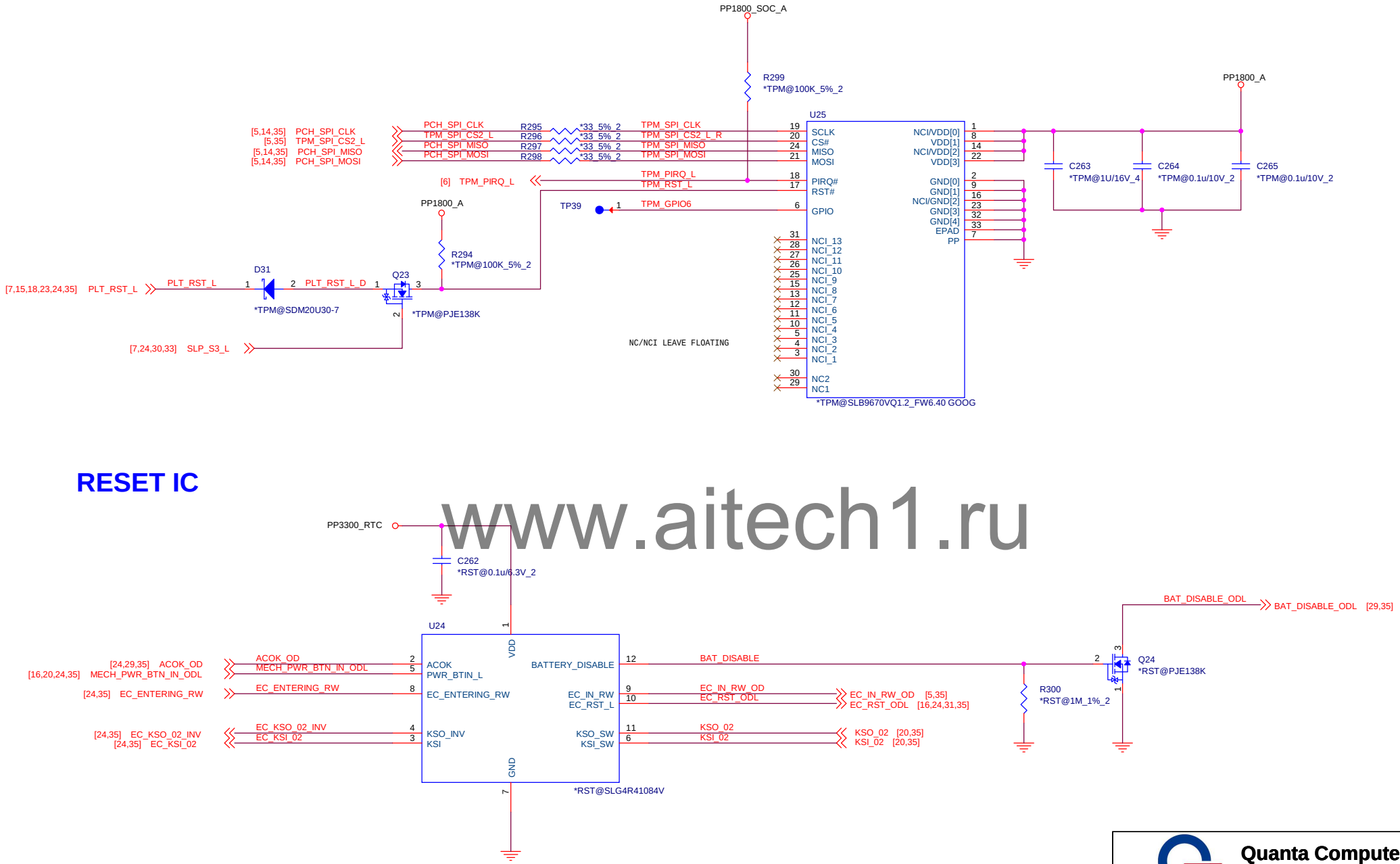
SERVO HEADER

Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number	Rev
	SERVO	1A
Date: Friday, July 28, 2017	Sheet 16 of 38	



RESET IC

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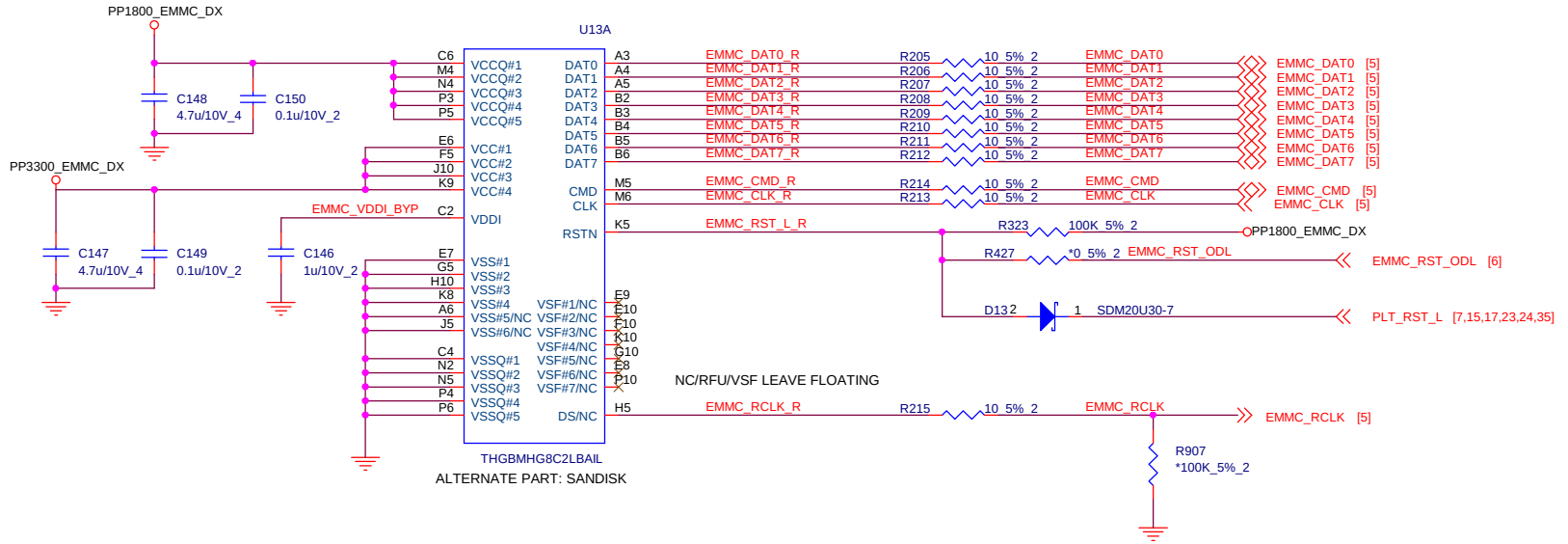
Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number	Rev
	TPM/SILEGO	1A
Date: Friday, July 21, 2017	Sheet 17 of 38	

32 GB EMMC SD STORAGE

150 UA SLEEP CURRENT



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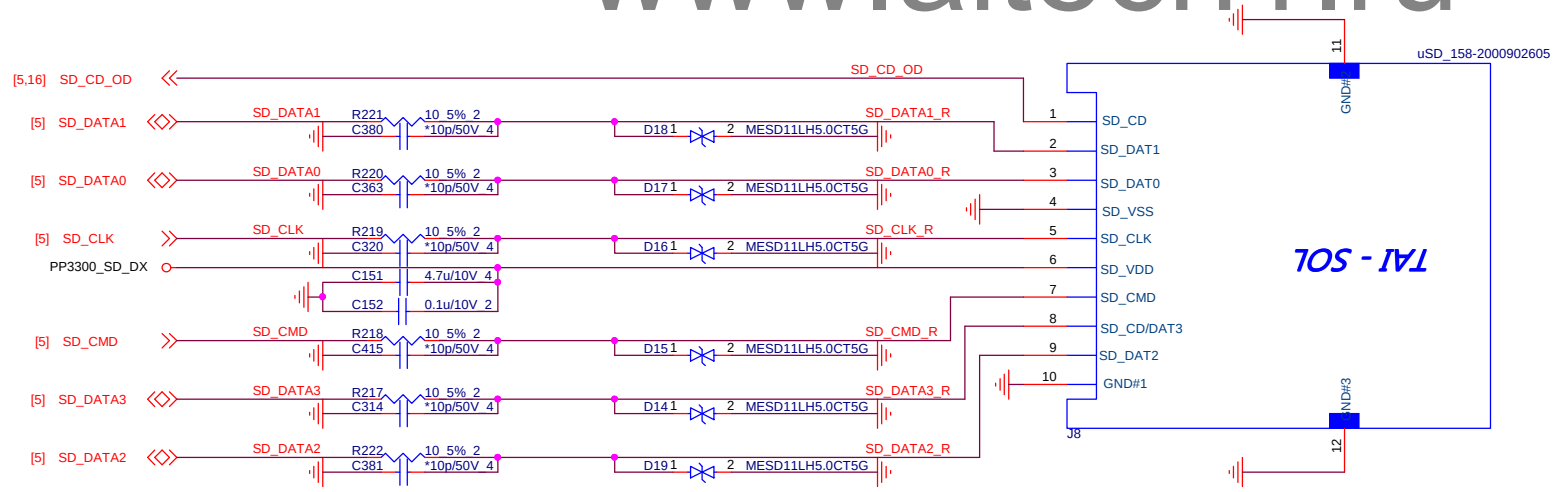
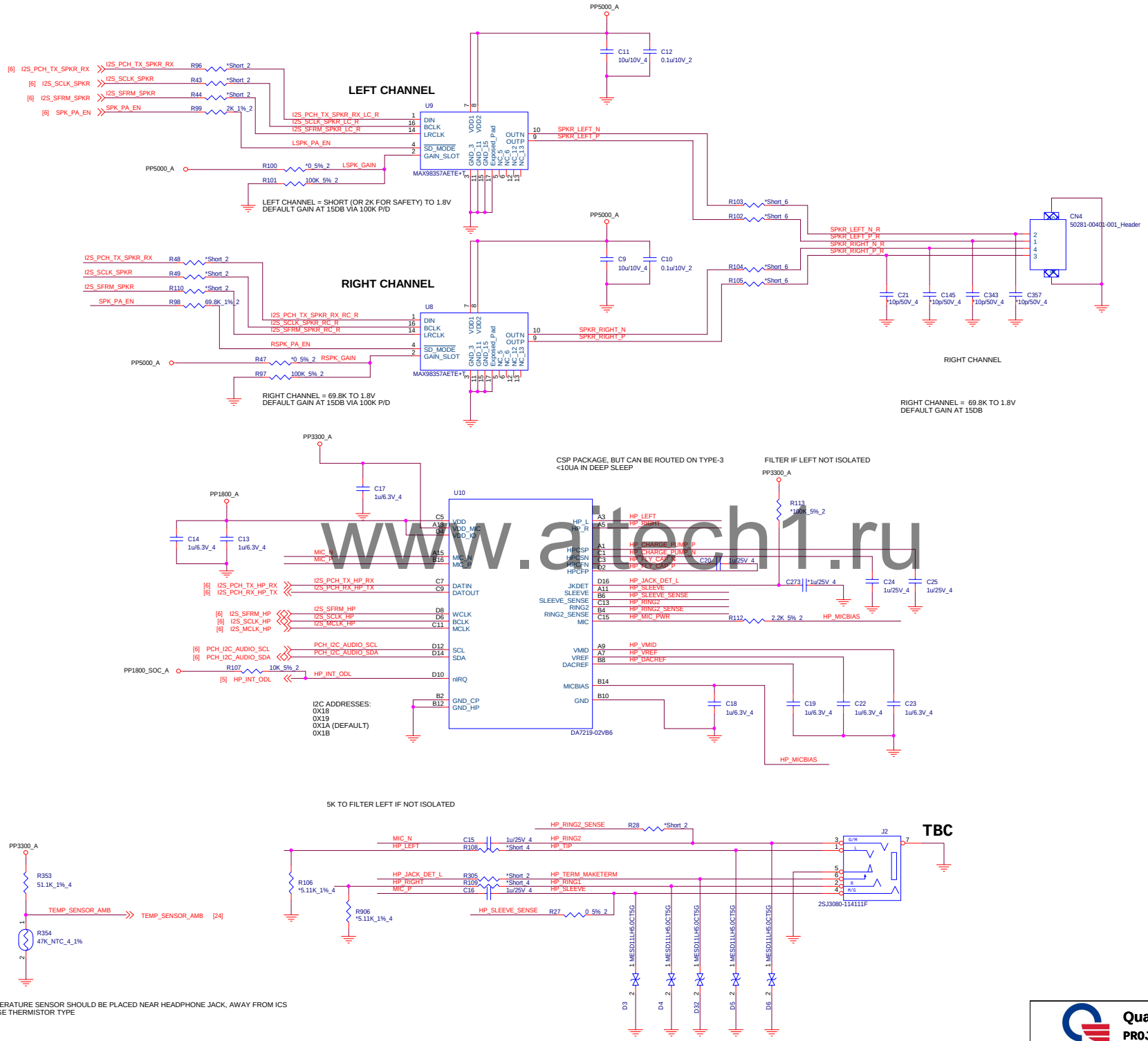
SD Connetcor



Quanta Computer Inc. PROJECT : ZRX		
Size	Document Number eMMC/SD	Rev 1A
Date: Friday, July 21, 2017	Sheet 18 of 38	



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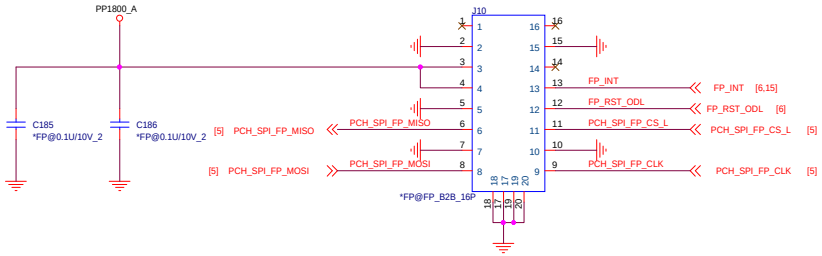
Quanta Computer Inc.			
PROJECT : ZRX			
Size	Document Number		Rev
	AUDIO		1A
Date: Friday, July 21, 2017	Sheet 19 of 38		

FINGER PRINT CONNECTOR

Not - Ready

Modify the pins assignment to meet Quanta's layout symbol rule.



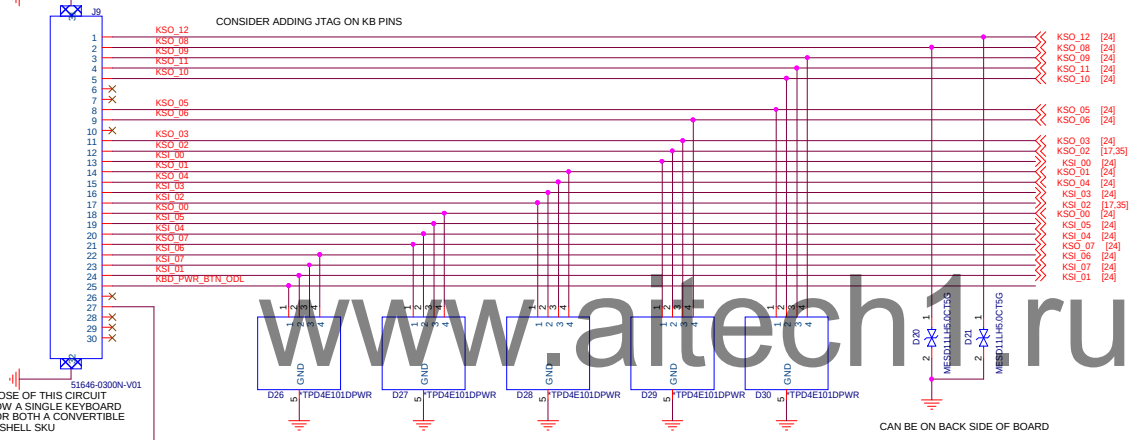
NFC CONNECTOR

SUBJECT TO CHANGE PER QUANTA REQUEST

Remove This Function

BSW REF DESIGN ERRATA MENTIONED
A LEAKAGE PROBLEM INTO THE EC
VIA THE KSO PINS. THE FIX WAS
TO ADD 100K PULLUPS TO 3P3A_EC
ON THE KSO SIGNALS
0C2A COMPATIBLE

CONSIDER ADDING JTAG ON KB PINS

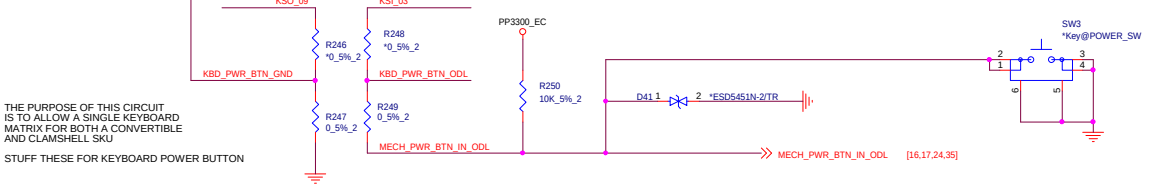


THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEYBOARD
MATRIX FOR BOTH A CONVERTIBLE
AND CLAMSHELL SKU

CAN BE ON BACK SIDE OF BOARD

STUFF THESE FOR KEYBOARD LOCK BUTTON

STUFF FOR POWER BUTTON (DETACHABLE)



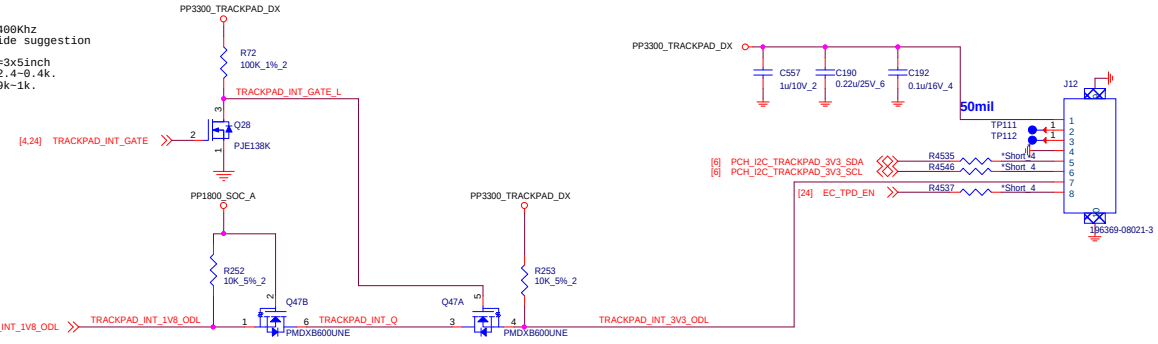
THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEYBOARD
MATRIX FOR BOTH A CONVERTIBLE
AND CLAMSHELL SKU

STUFF THESE FOR KEYBOARD POWER BUTTON

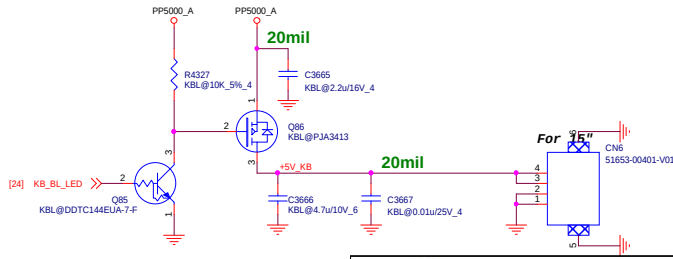
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

(TPD)

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.



KB_BL Control



11/3/16

Remove Pen connector
Add KB backlight circuit

Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	BASE: KB, TP, NFC, FINGER	1A
Date: Friday, July 21, 2017	Sheet 20 of 38	

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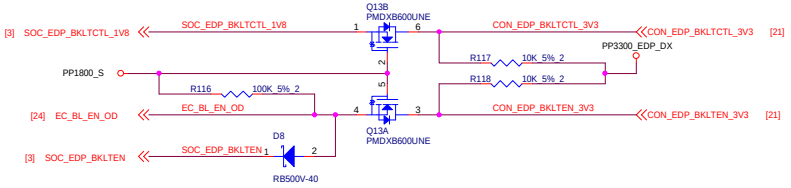
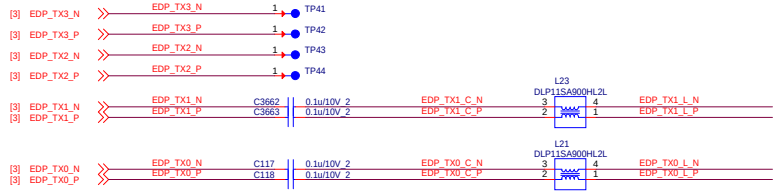
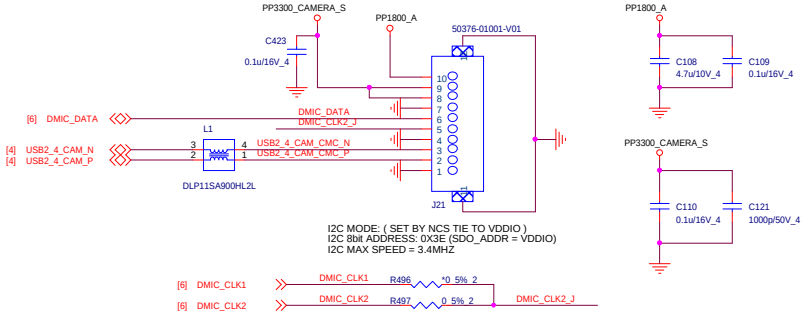
EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR





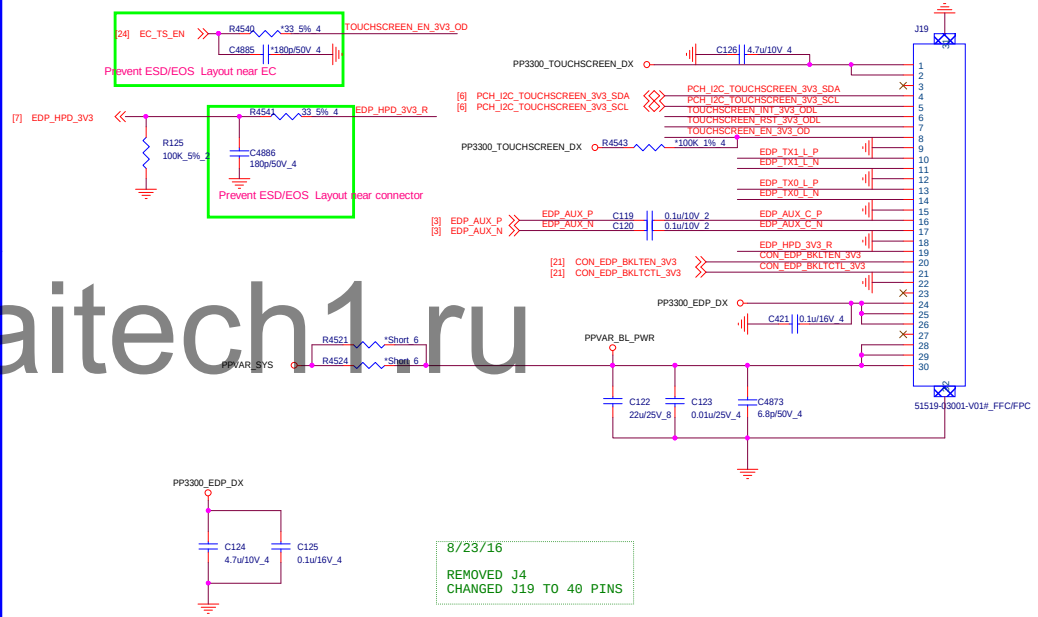
CCD/DMIC BOARD (KX022+DMIC)



Sensor I2C Level shift

Remove This Function

EDP + TouchScreen Connector



8/23/16

REMOVED J4
CHANGED J19 TO 40 PINS

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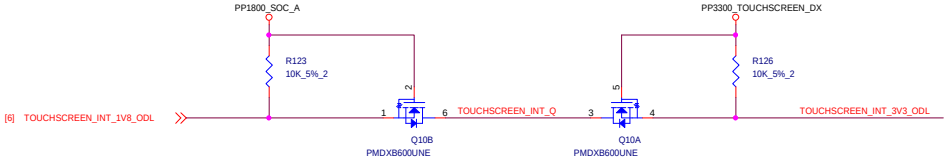
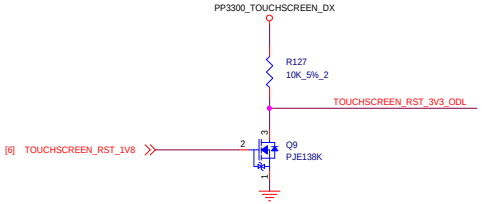
TOUCH SCREEN



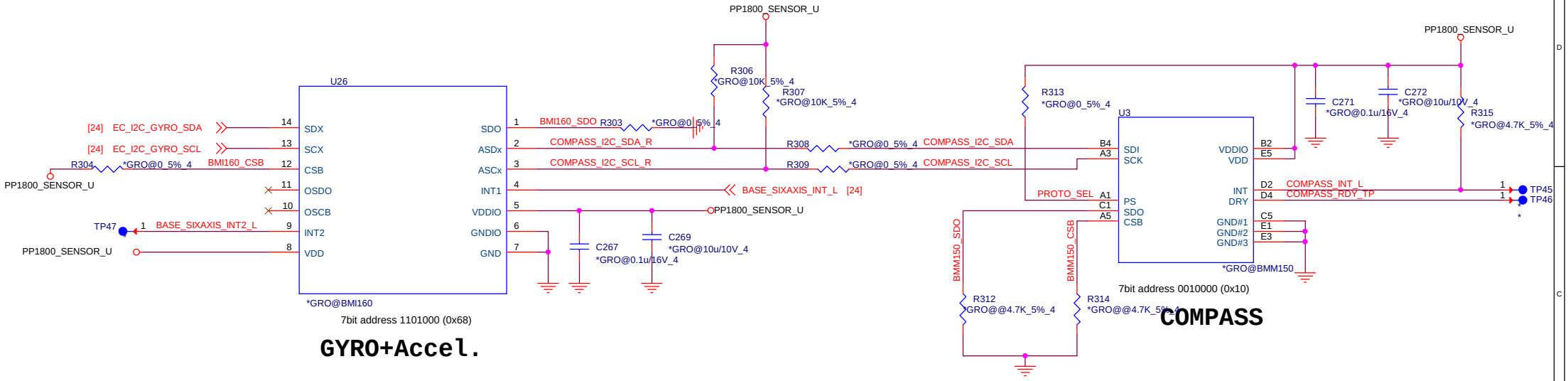


C-PANEL CAMERA

Remove This Function

Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	LID: eDP, CAM, TOUCH, SEN	1A
Date: Friday, July 21, 2017	Sheet 21 of 38	



BAROMETER

Remove This Function

CHARGE/BATTERY LED

TO Sub Board

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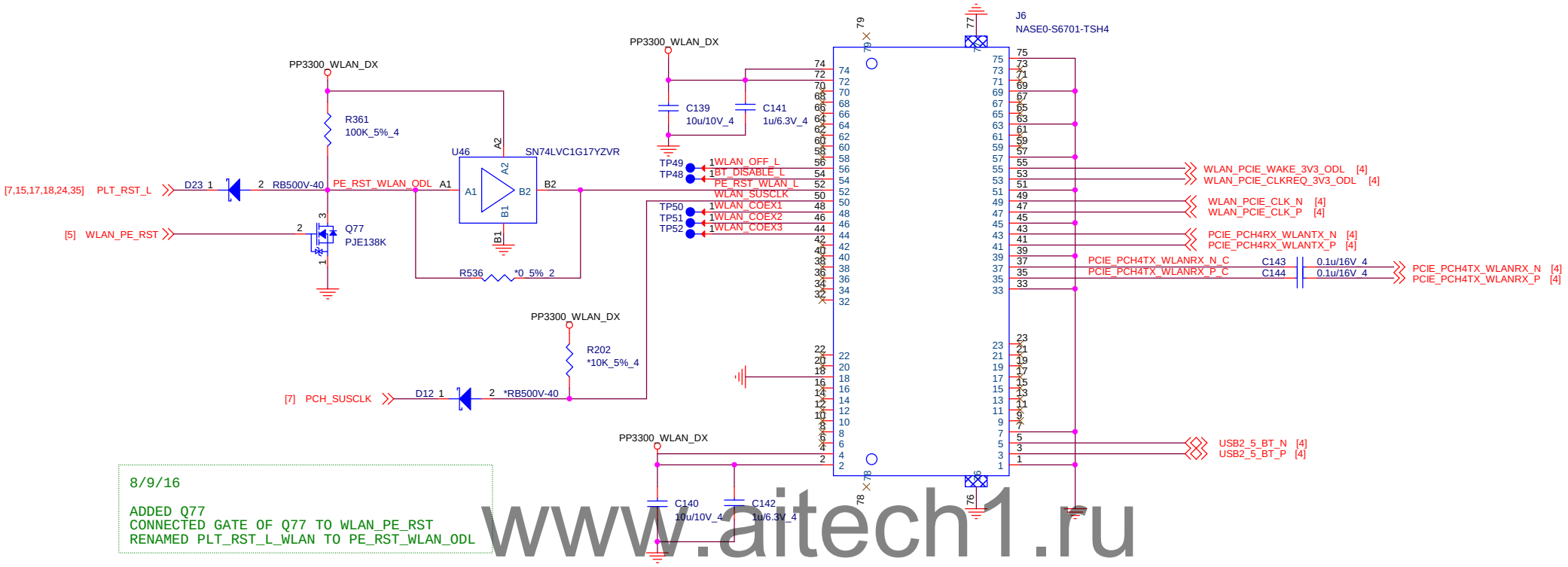
Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: COMPASS, BARO, GYRO, LID	Rev: 1A
Date: Friday, July 21, 2017	Sheet 22 of 38	

M.2 connector (Wifi+BT)



8/9/16

ADDED Q77
CONNECTED GATE OF Q77 TO WLAN_PE_RST
RENAMED PLT_RST_L_WLAN TO PE_RST_WLAN_ODL

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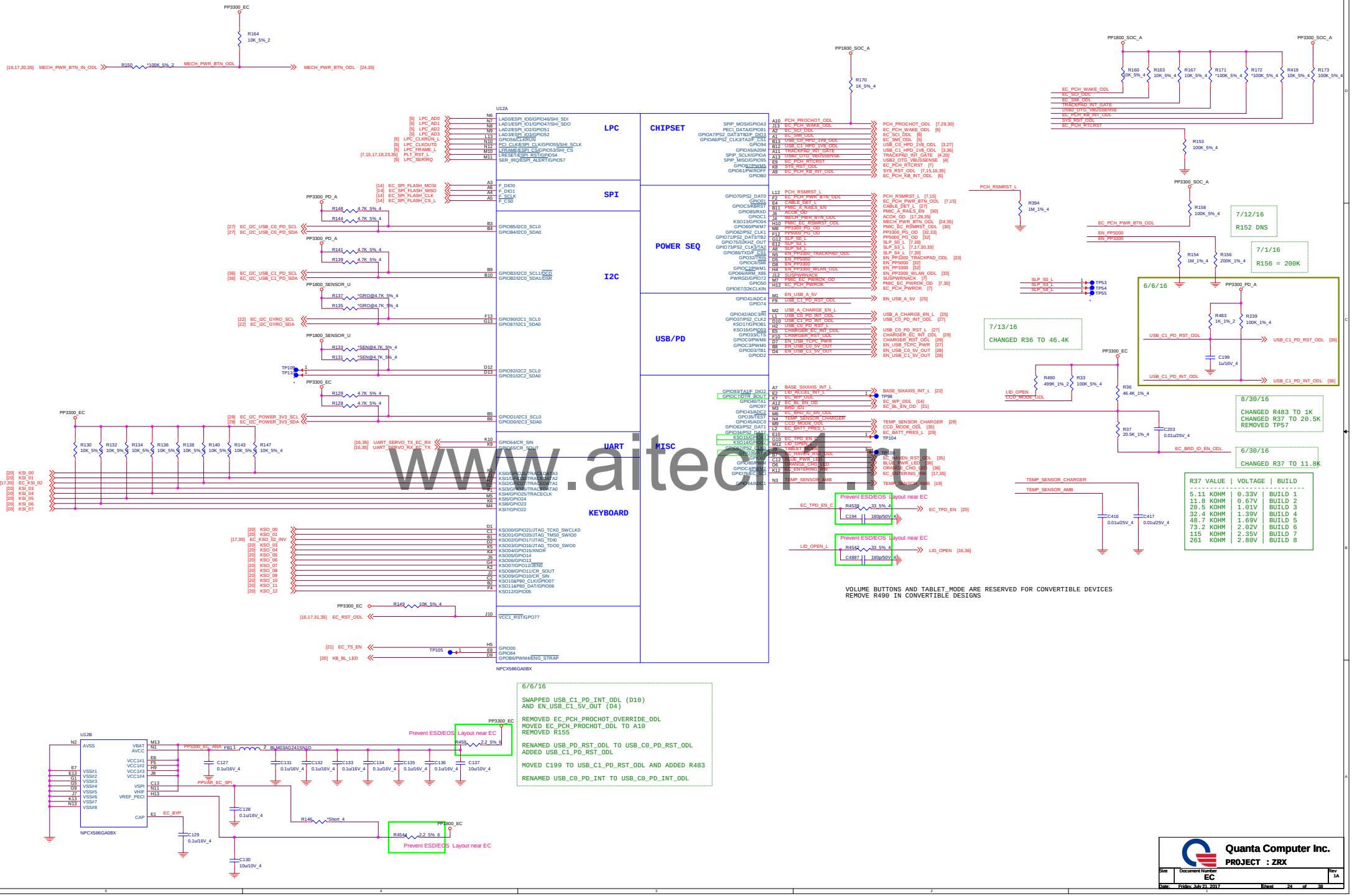
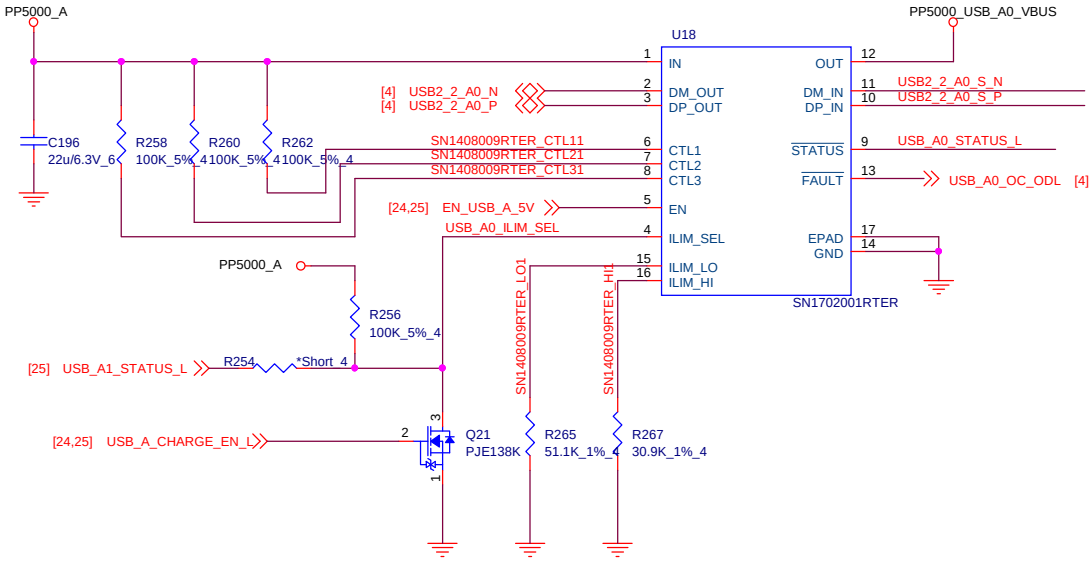
GPS connector

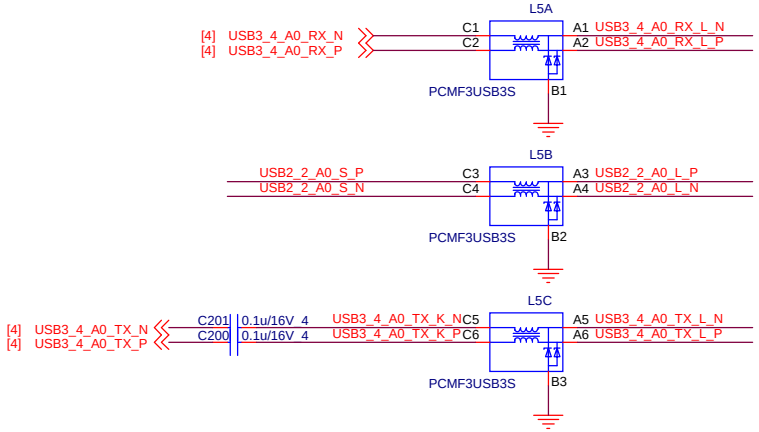
Remove This Function

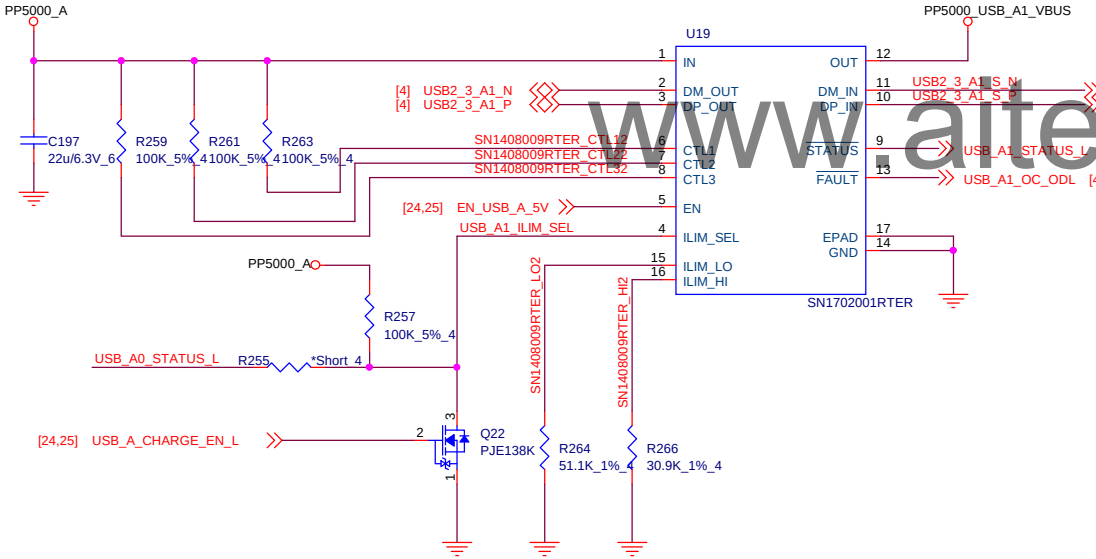
Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: WIFI,GPS CONNTECOR	Rev: 1A
Date: Friday, July 21, 2017	Sheet 23 of 38	

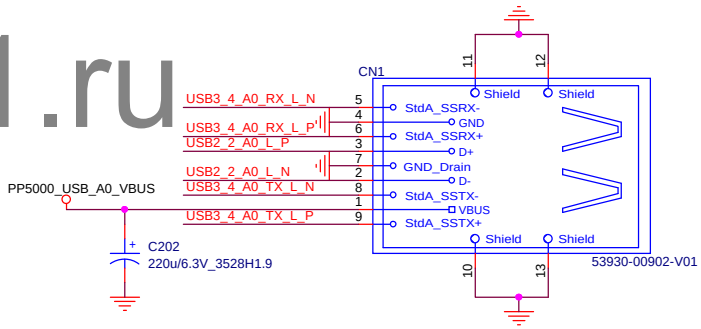


www.aitech.ua









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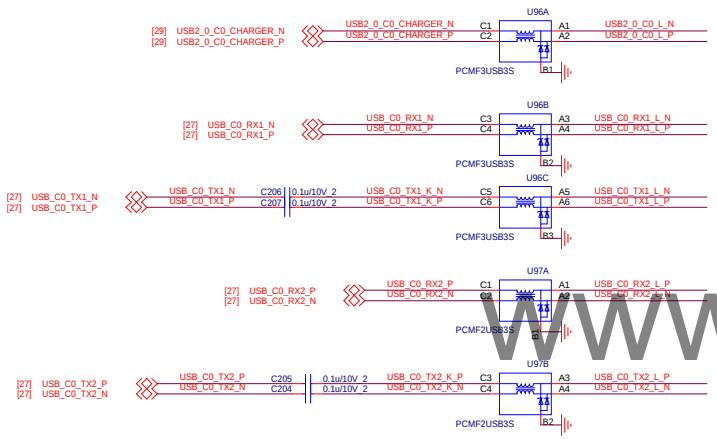
Quanta Computer Inc.

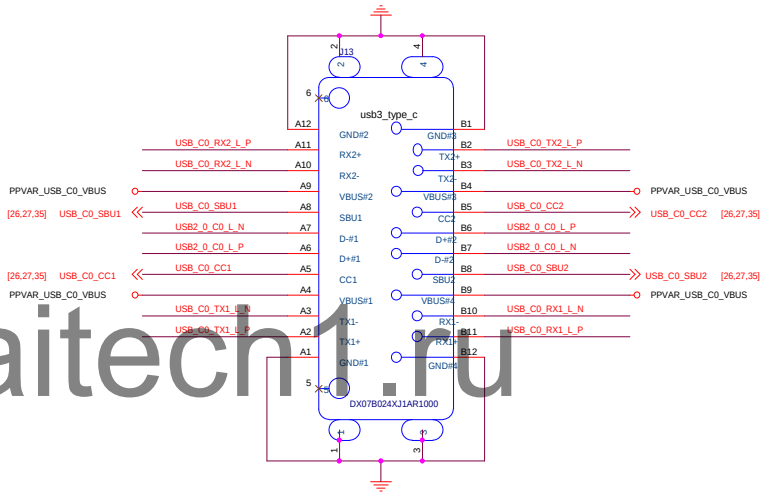
PROJECT : ZRX

Size	Document Number	Rev
	USB A CONNECTORS	1A

Date: Friday, July 21, 2017 Sheet 25 of 38

PORT 0 TYPE-C MLB





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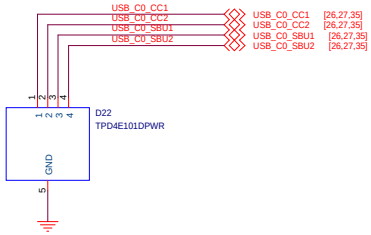
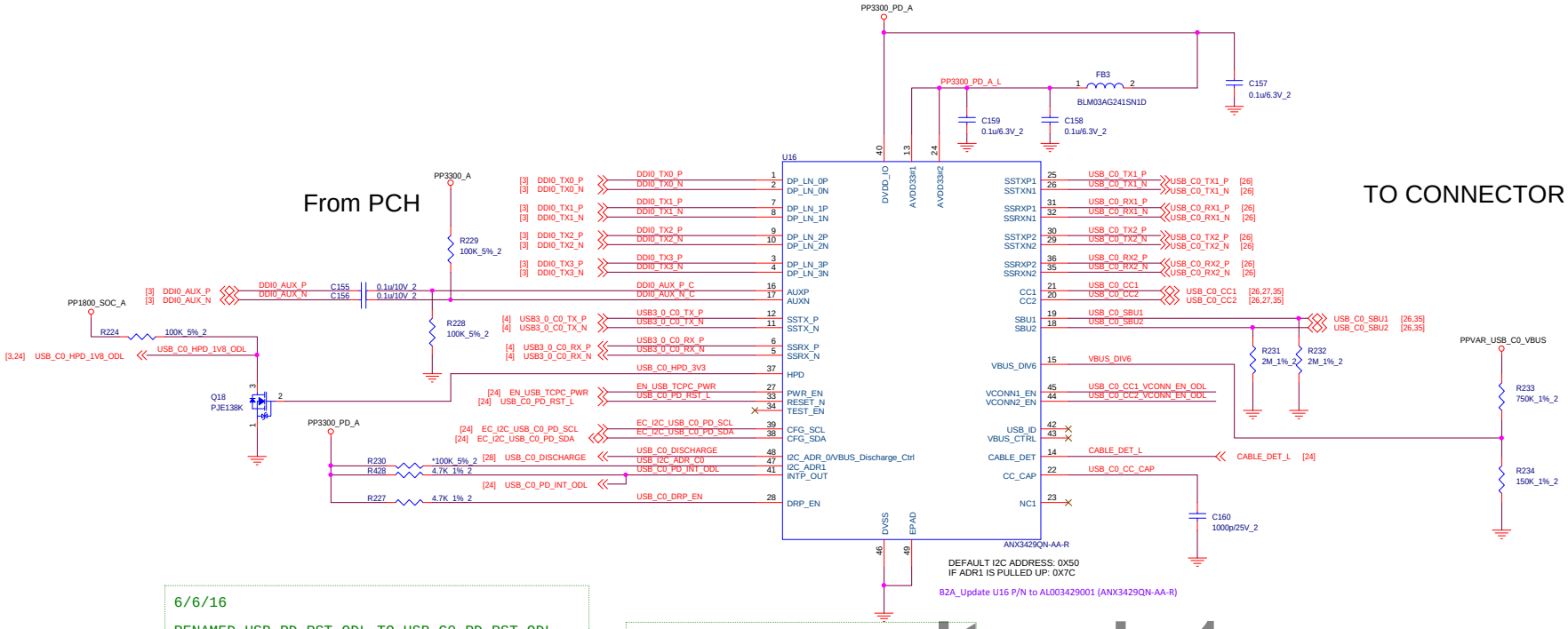
ESD Protection



Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	USB C CONNECTORS	1A
Date: Friday, July 21, 2017	Sheet 26 of 38	



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Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: USB C TCPC/MUX	Rev 1A
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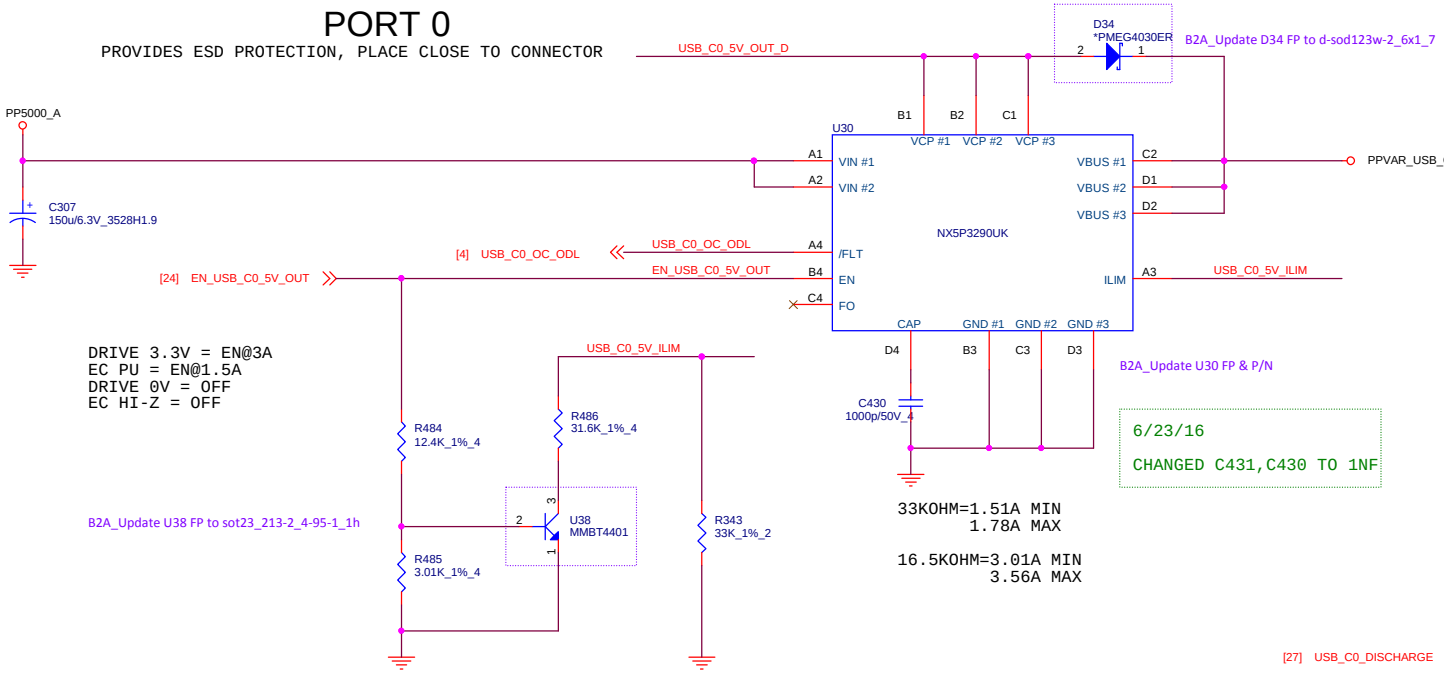
PORT 0

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR



DRIVE 3.3V = EN@3A
EC PU = EN@1.5A
DRIVE 0V = OFF
EC HI-Z = OFF

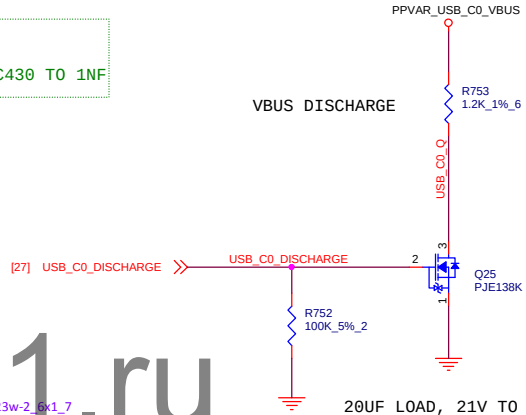
33KOHM=1.51A MIN
1.78A MAX

16.5KOHM=3.01A MIN
3.56A MAX

6/23/16

CHANGED C431,C430 TO 1NF

VBUS DISCHARGE



20UF LOAD, 21V TO <0.8V IN <80MS
20UF LOAD, 5V TO <0.8V IN <45MS
0402 CAN DISSIPATE 400MW FOR 80MS
0603 CAN DISSIPATE 400MW FOR 500MS
0805 CAN DISSIPATE 400MW FOR 2000MS

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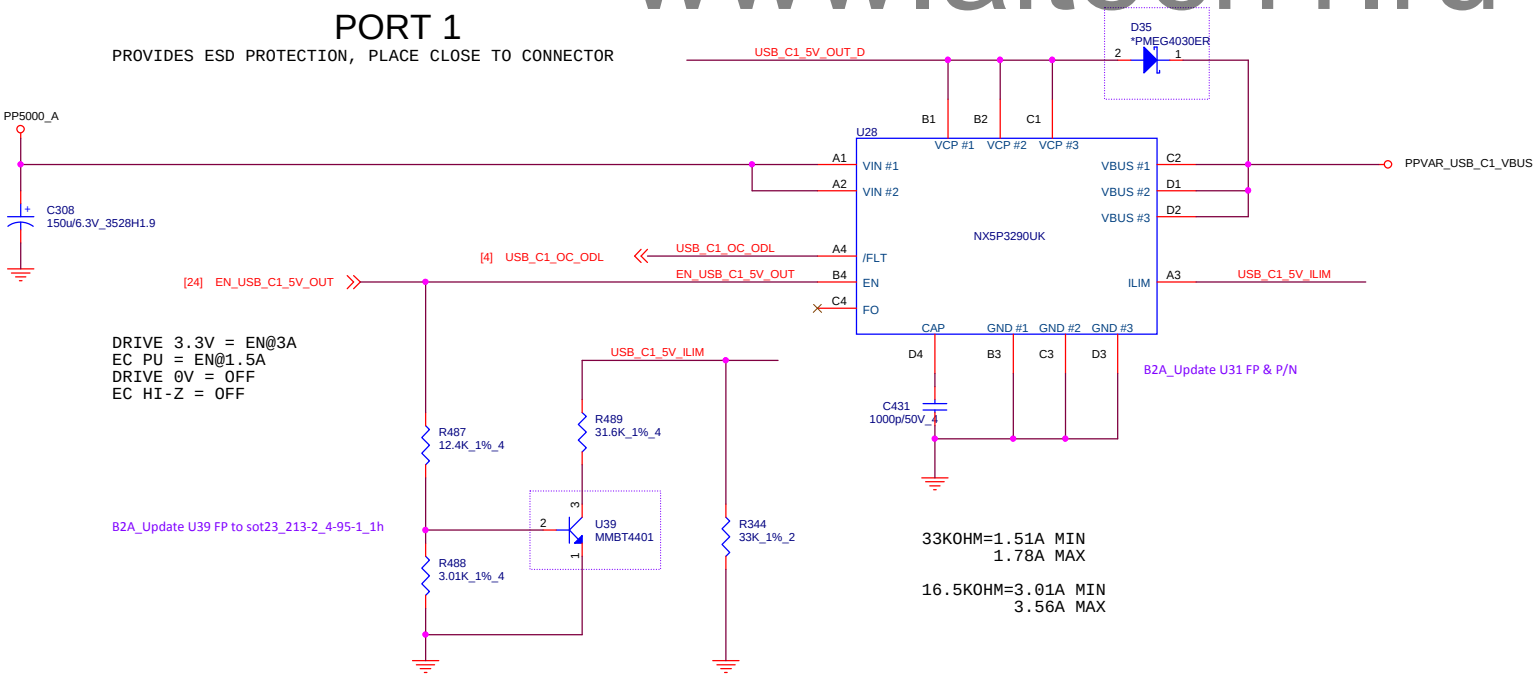
PORT 1

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR



DRIVE 3.3V = EN@3A
EC PU = EN@1.5A
DRIVE 0V = OFF
EC HI-Z = OFF

33KOHM=1.51A MIN
1.78A MAX

16.5KOHM=3.01A MIN
3.56A MAX

Quanta Computer Inc.
PROJECT : ZRX

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	USB C 5V OUT	1A
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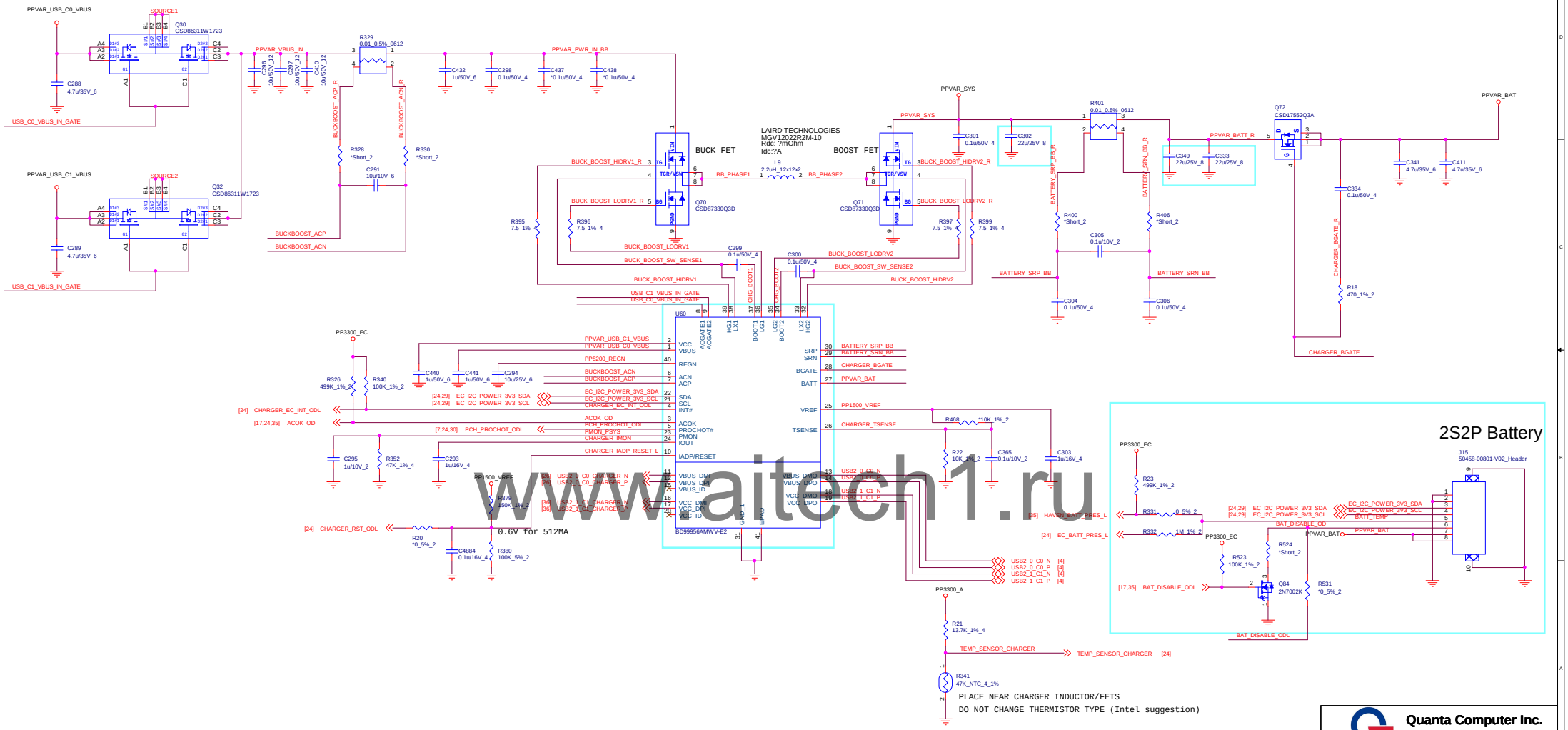
POWER - BATTERY CHARGER

ROHM BUCK-BOOST CHARGER



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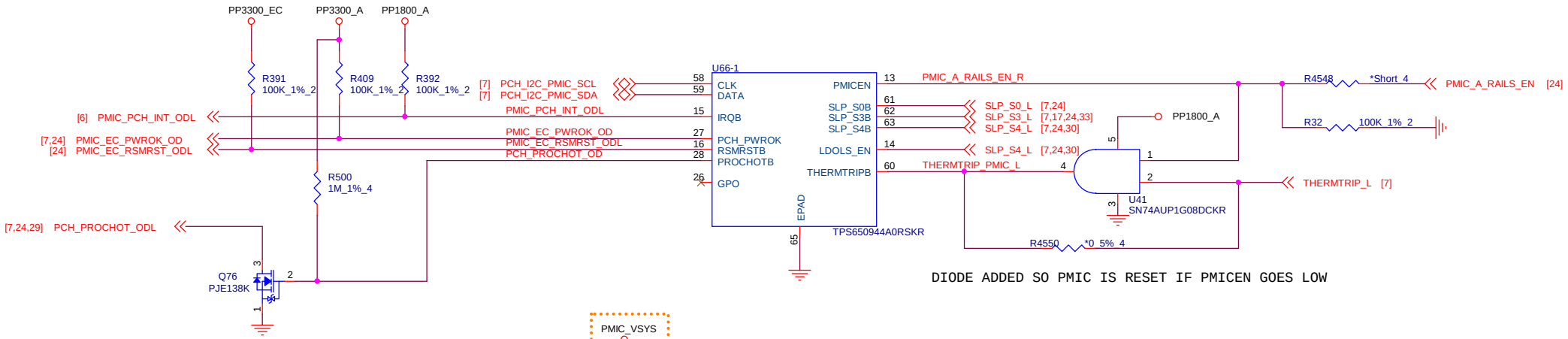
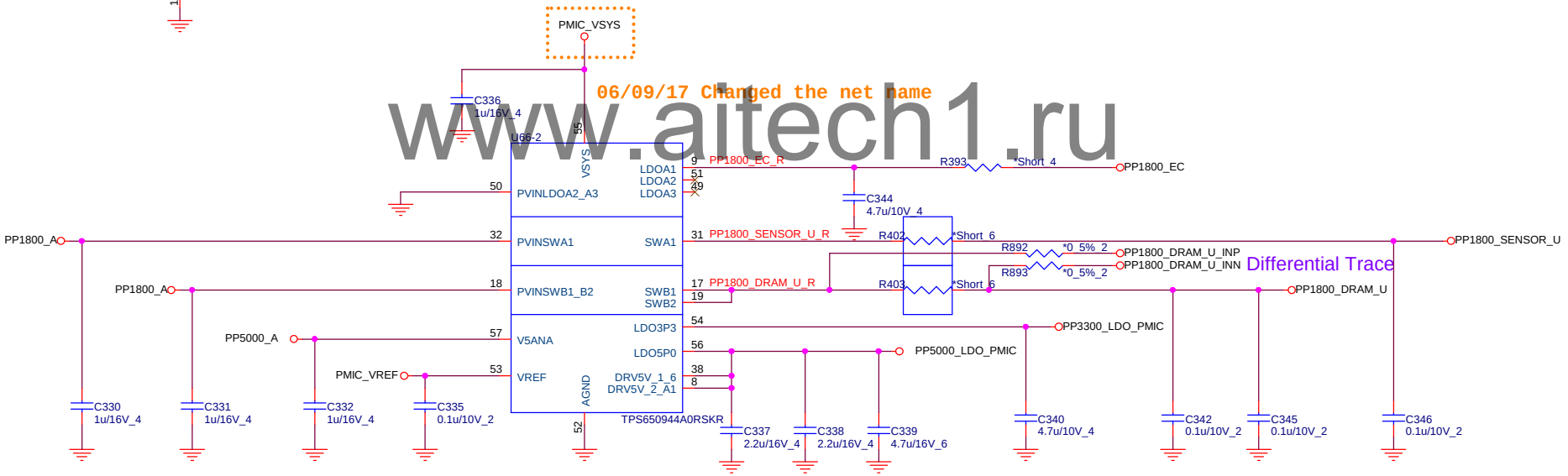
Quanta Computer Inc.			
PROJECT : ZRX			
Size	Document Number		Rev
	POWER - BATTERY CHARGER		1A
Date: Friday, July 21, 2017		Sheet 29 of 38	

POWER - PMIC LOGIC



DIODE ADDED SO PMIC IS RESET IF PMICEN GOES LOW



4.7UF ON LDO5P0
2.2UF ON DRV5V5_1_6
2.2UF ON DRV5V_2_A1

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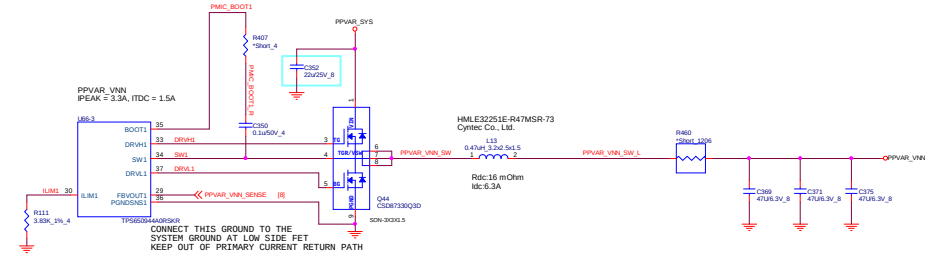
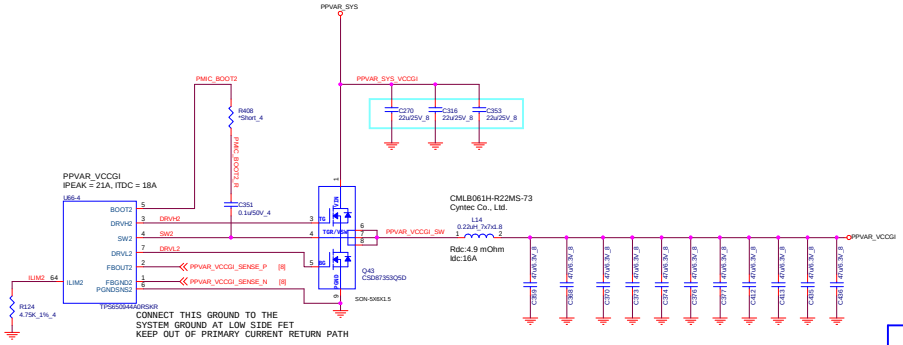
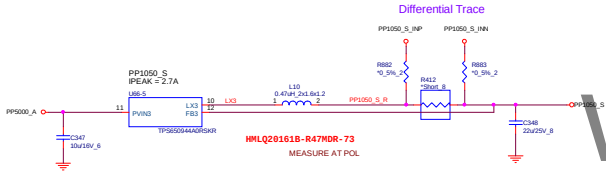
Quanta Computer Inc.
PROJECT : ZRX

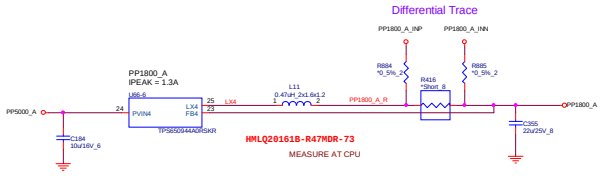
Size	Document Number	Rev
	POWER - PMIC LOGIC	1A
Date: Friday, July 21, 2017	Sheet 30 of 38	

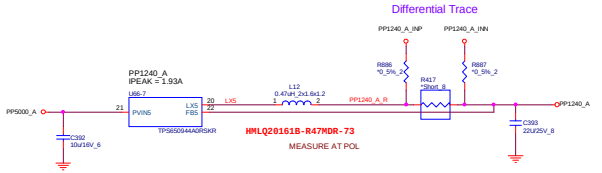
POWER - PMIC RAILS

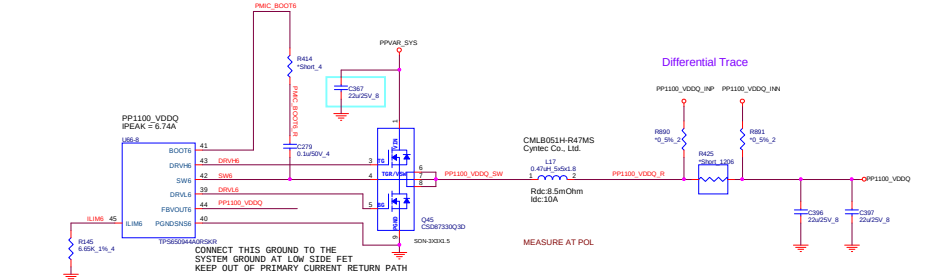




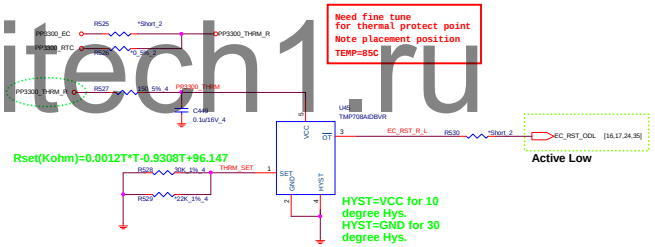






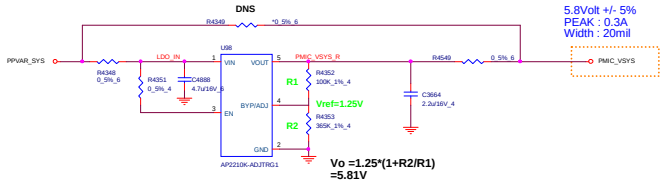


Thermal Protector



PMIC_VSYS

06/09/17 Add AP2210



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Quanta Computer Inc.
PROJECT : ZRX
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POWER - PMIC RAILS
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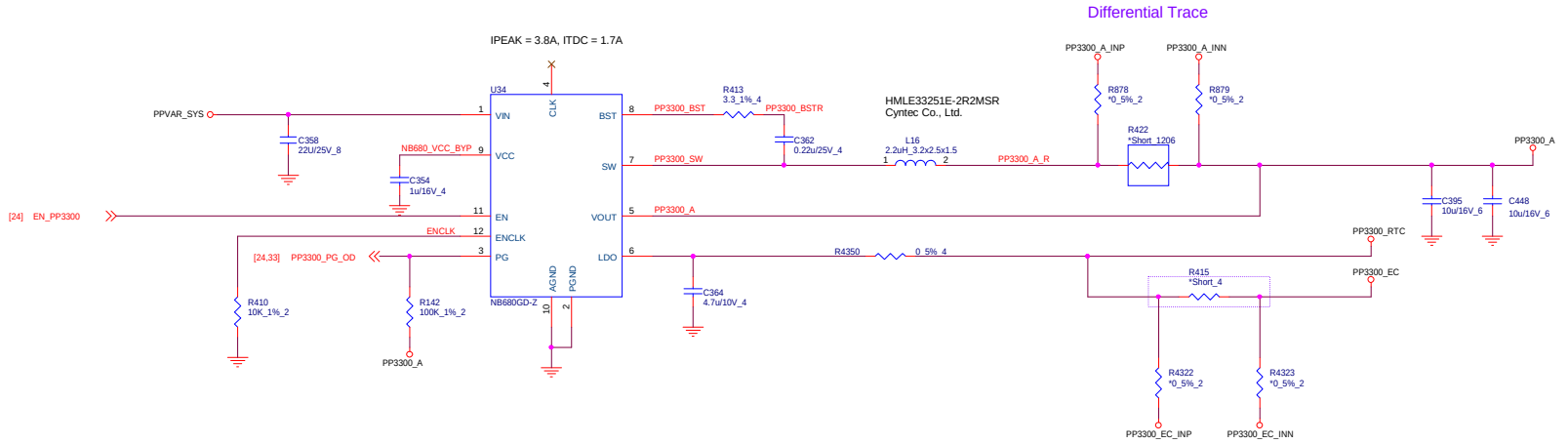
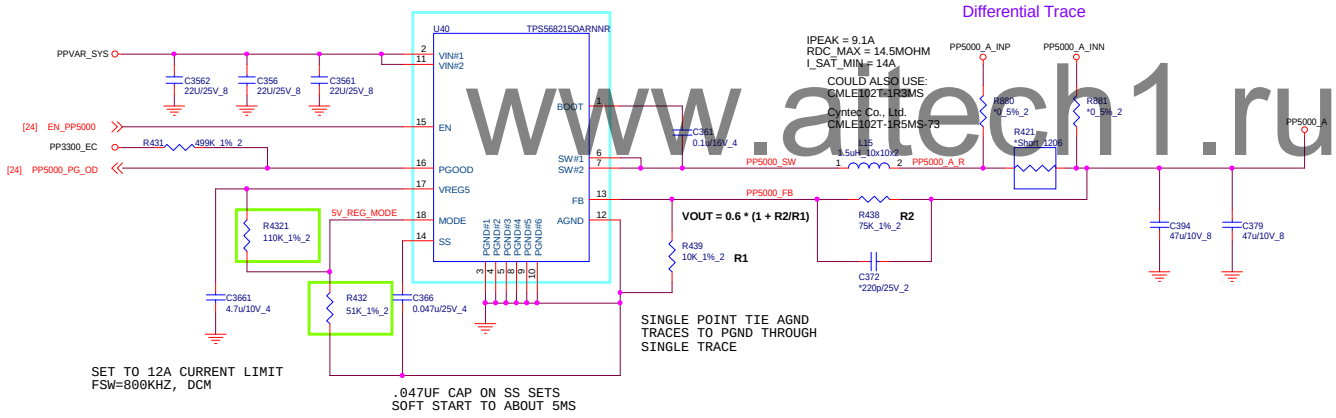
PP3300_A



PP5000_A



7/1/16

Fixed note to say "Soft start to about 5ms"

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Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	POWER: 3.3V AND 5V	1A
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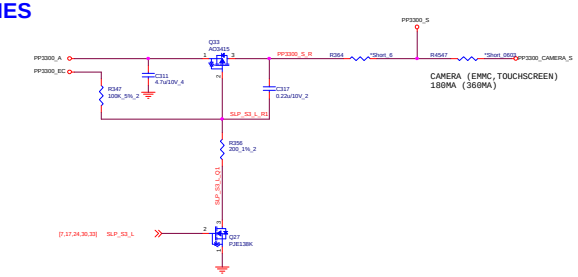
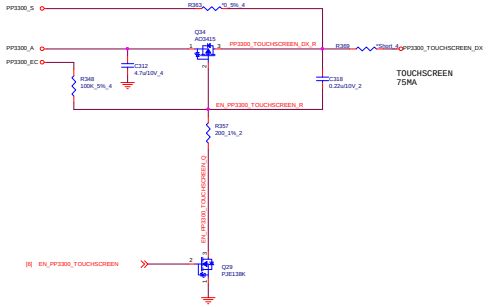
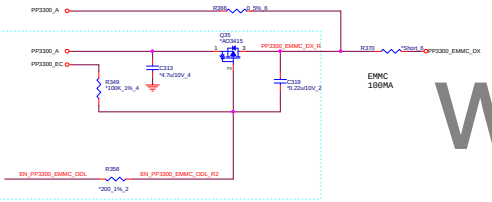
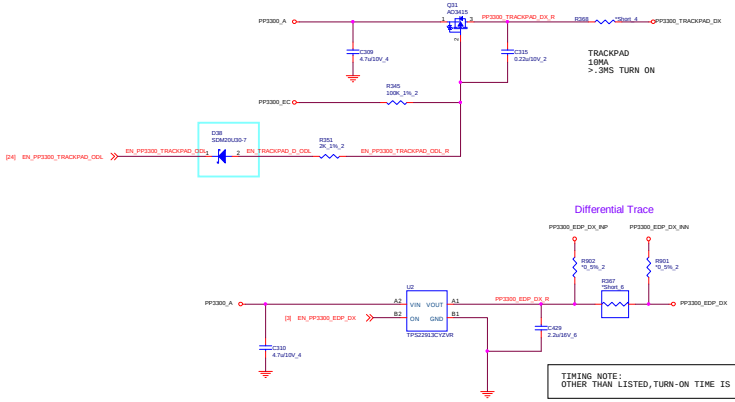
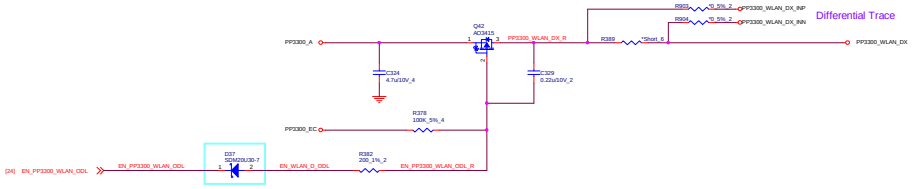
POWER - LOAD SWITCHES

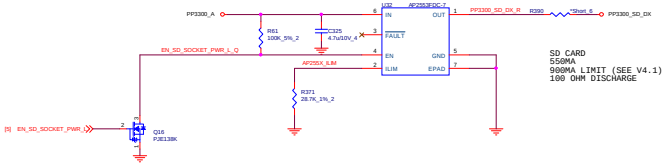


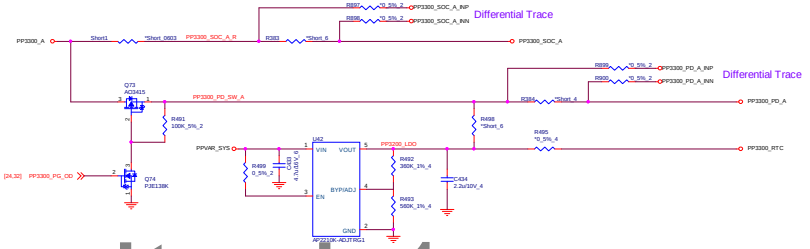


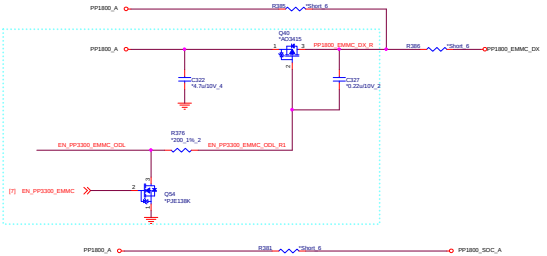


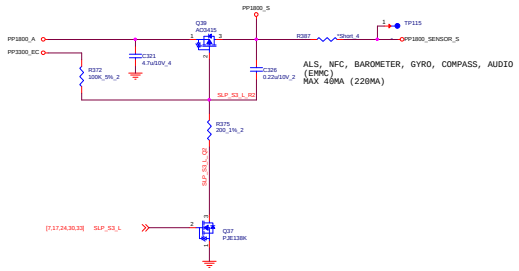












PP1800_A RAIL

NFC

Remove This Function

PP5000_A RAIL

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Quanta Computer Inc.
PROJECT : ZRX
POWER - LOAD SWITCHES
Rev 1A
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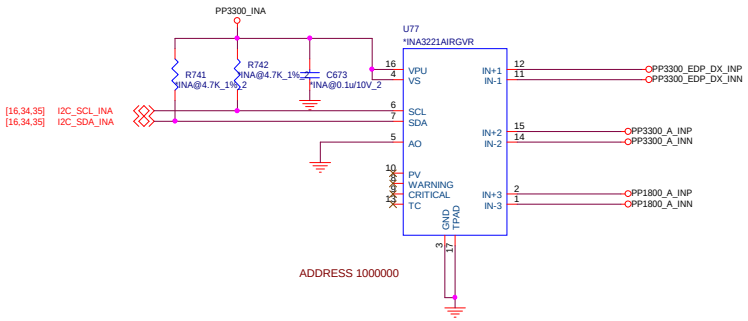
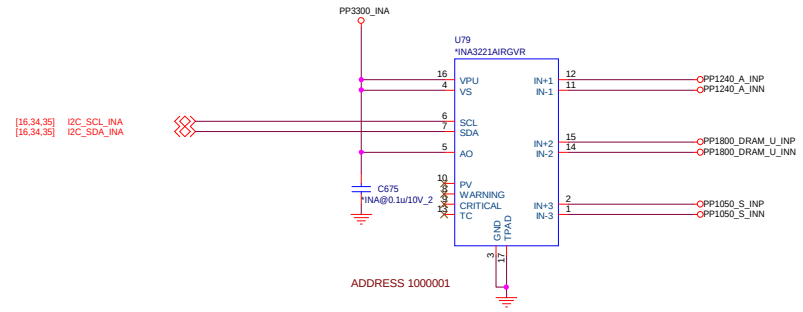
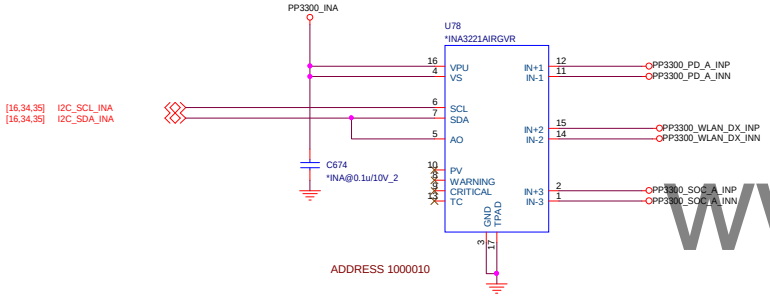
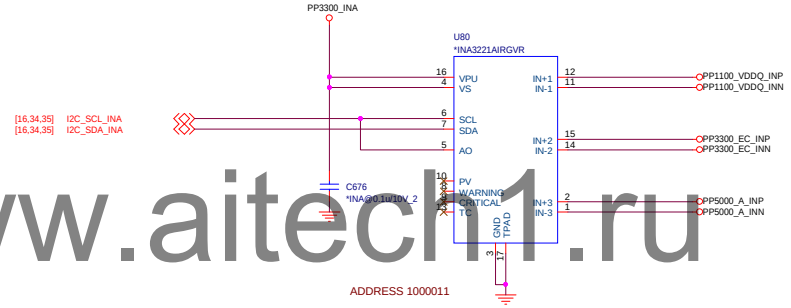
INAs









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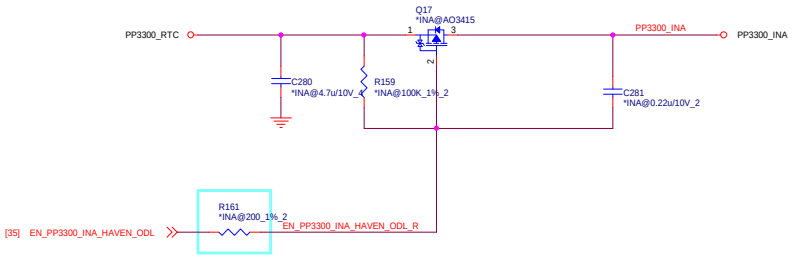
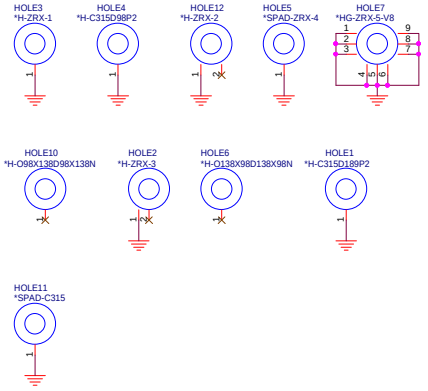
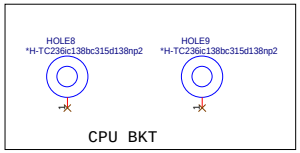


HOLES

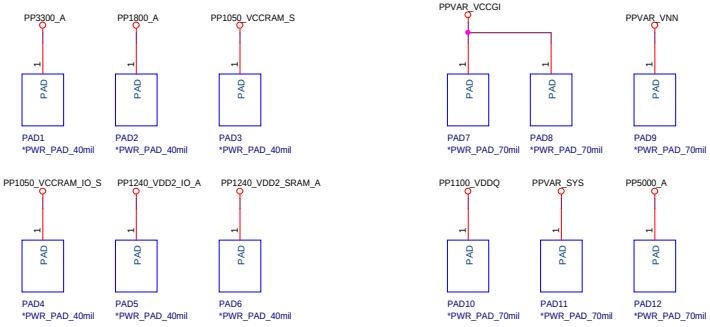




POWER TEST PAD

6/6/16
Remove solder mask on PAD 1 - PAD12

6/29/16
Add solder mask on PAD 1 - PAD12



Quanta Computer Inc.
PROJECT : ZRX

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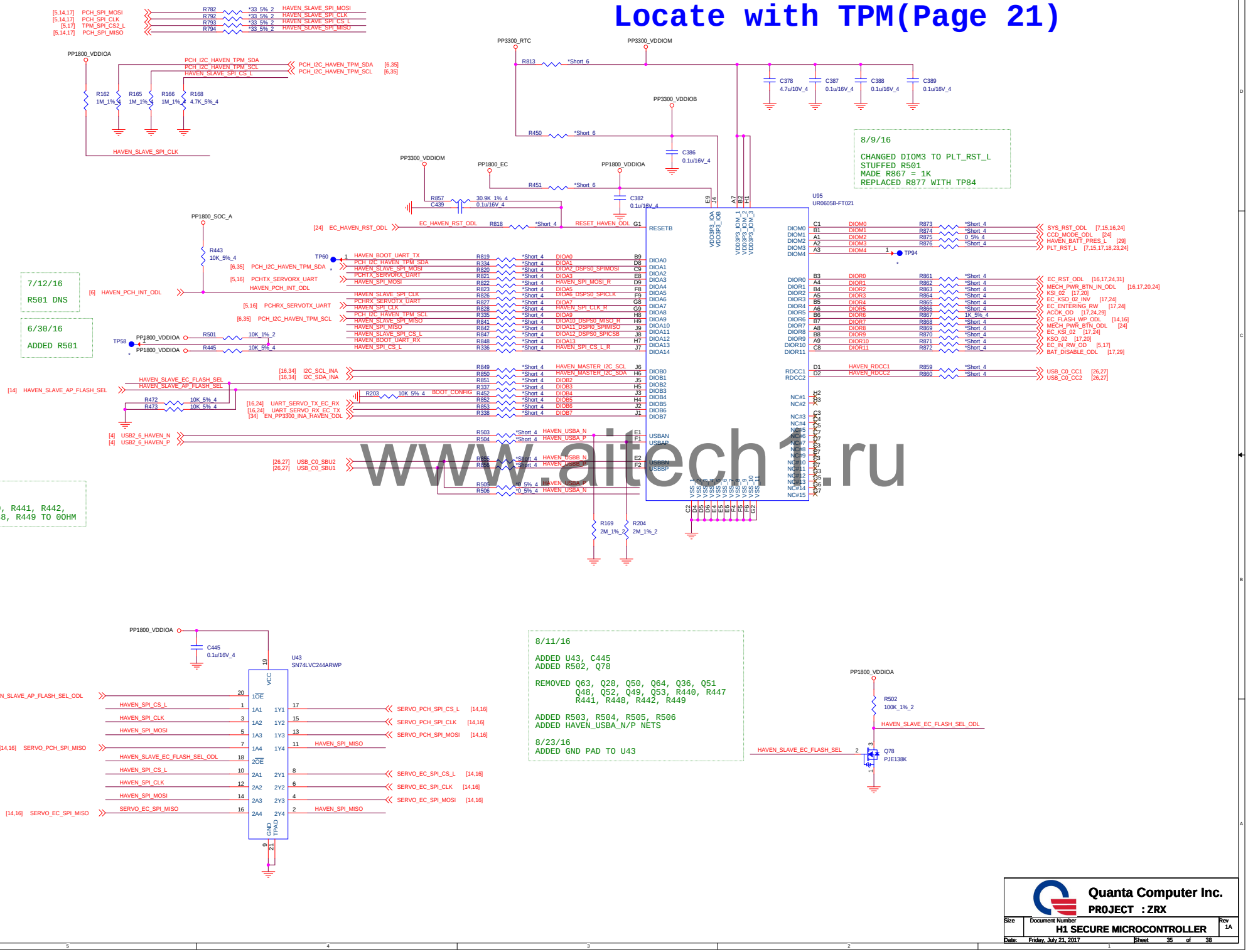
Locate with TPM(Page 21)



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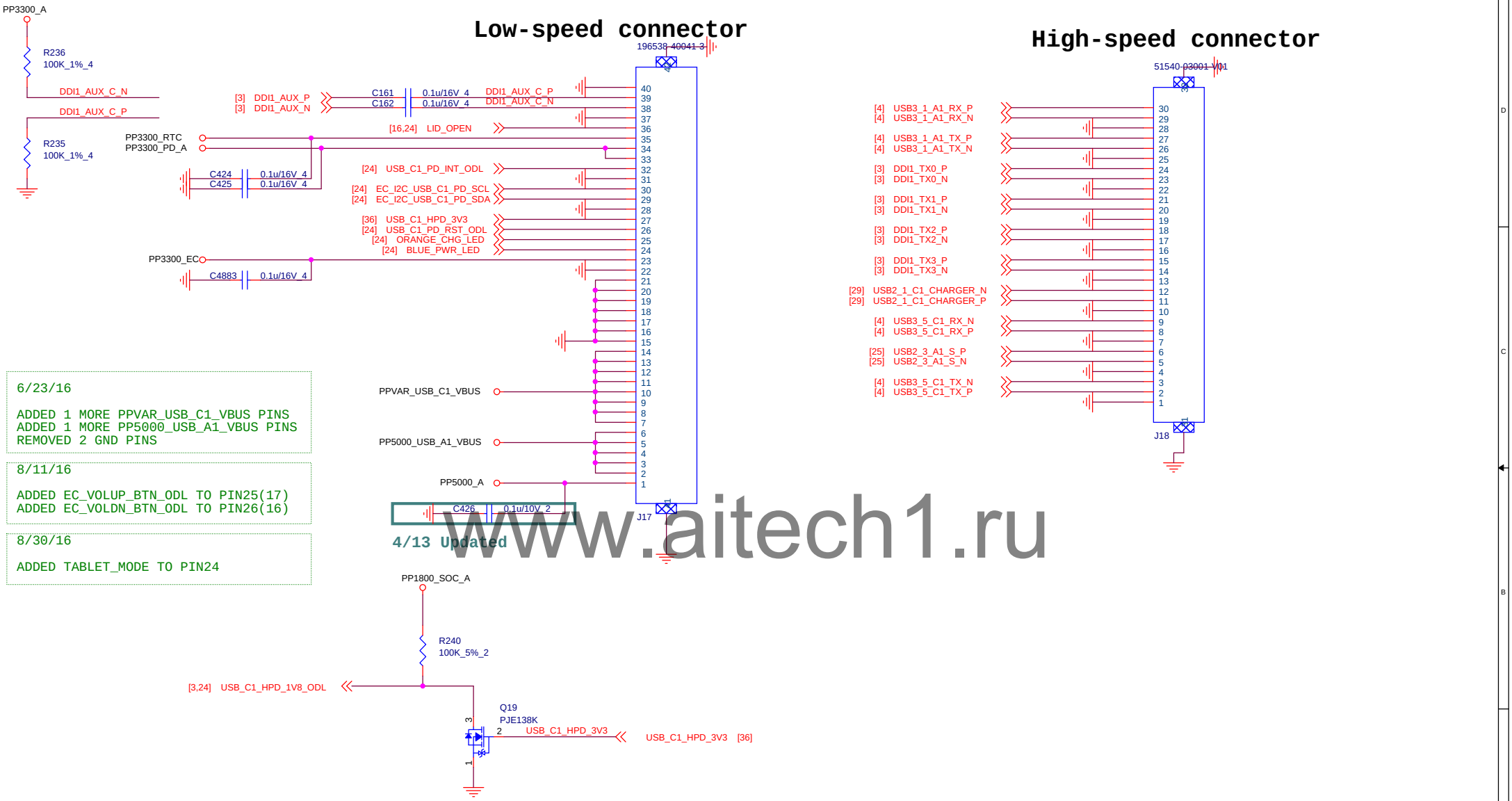

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Quanta Computer Inc.		
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Size	Document Number	Rev
	MLB CONNECTORS	1A
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Model	Version	CHANGE LIST
ZRX	B	2017/3/7 page 20 Change U18 U19 P/N to SN1702001RTER page 23 Change J6 footprint to ngff-nase0-s6701-tsh4-ke-smt 2017/3/9 page 24 Change R37 from 5.11K ohm to 11.8K ohm for Build 2 page 31 Change R528 to 30Kohm for thermal protect when temp is 76.3C page 20 Change U18 U19 P/N to SLGC55545VTR page 36 Change J18 P/N form DFFC30FR181 to DFFC30FR172
	C	2017/4/6 page 29 DNI R20 , Add C4884 0.1uF Cap to GND on CHARGER_IADP_RESET_L page 06 Changed R38 and R39 pull-up value to 1K 2017/4/11 page 24 Add EOSD/ESD solution (R4539 33ohm and C194 180pF) on EC_TPD_EN Change EC_TS_EN from EC_GPIO83 to EC_GPIO00 Add EOSD/ESD solution (R4542 33ohm and C4887 180pF) on LID_OPEN page 21 Change EC_TS_EN from J19 Pin23 to J19 Pin8 , Add EOSD/ESD solution (R4540 33ohm and C4885 180pF) on EC_TS_EN Add EOSD/ESD solution (R4541 33ohm and C4886 180pF) on EDP_HPD_3V3 Add pull High Registor (R4543 100k ohm) on TOUCHSCREEN_EN_3V3_OD page 20 Add ESD solution (D41) on MECH_PWR_BTN_IN_ODL page 24 Change R37 to 20.5K (BUILD 3) 2017/4/12 page 24 Add EOSD/ESD solution (R459 2.2ohm and R4544 2.2ohm) on Embed Controller Power (U12.M13/U12.N1 and U12.C13/U12.H13 page 07 change Q79,Q81,Q82 P/N to PJA3413 2017/5/04 page 21 DNI R4543 2017/5/11 page 20 DNI SW3 (Hardware power Key) 2017/5/15 Change 0-ohm to short pad page 04 R12,R13,R14,R15 page 05 R281 page 08 R461,R462,R463,R464 page 14 R77,R78,R79,R80,R84,R85,R86,R87 page 15 R180~R187,R174,R200 page 19 R96,R43,R44,R48,R49,R110,R102,R103,R104,R105,R28,R108,R305,R109 page 20 R4535,R4536,R4537 page 21 R4521,R4524 page 24 R146 page 25 R254,R255 page 29 R328,R330,R400,R406,R524 page 31 R407,R408,R414,R525,R530 page 33 R498 page 35 R813,R818 ~ R823,R826,R827,R828,R841,R842,R847 ~ R853,R855,R856,R334 ~ R338,R450 ~ R452,R503,R504,R873,R874,R876,R859 ~ R866,R869~R872 2017/5/17 Change milli-ohm to short pad page 30 R393/0.51ohm 2017/5/18 DNI INAs Function page 16 Q68,Q69,Q75,C442,C443 page 30 R892,R893 page 31 R882,R883,R884,R885,R886,R887,R890,R891 page 32 R878,R879,R880,R881,R4322,R4323 page 33 R897,R898,R899,R900,R901,R902,R903,R904 Change milli-ohm to short pad page 30 R402/0.02ohm,R403/0.02ohm page 31 R460/0.002,R412/0.01,R416/0.02,R417/0.02,R425/0.002 page 32 R422/0.002,R415/0.51,R421/0.002 page 33 R364/0.02,R367/0.02,R368/0.1,R369/0.1,R370/0.02,R381/0.02,R383/0.02,R384/0.1,R386/0.02,R387/0.1,R389/0.02,R390/0.02 2017/5/24 ADD PMIC Power Issue Debug page 30 Add R4548, R4348 0 ohm resistor and change R393 to 0 ohm. page 31 Add R4350 0 ohm resistor. 2017/6/02 page 25 Change U18,U19 P/N to TI-SN1702001RTER 2017/6/12 page 30 Change the net name at 55 pin of PMIC to PMIC_VSYS. page 31 Add U98 group for PMIC issue in PMIC_VSYS
	Ramp	2017/6/15 page 30 Add R4550 bypass to avoid U41 Logic unit

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Model	Version	CHANGE LIST
ZRX	C Ramp	2017/6/19 page 6 Add R4538 on GP_15 for S3 issue. It can using TP to wake up on S3 2017/6/19 Change 0-ohm to short pad page 30 R4548 ,R393 page 33 R385 2017/7/28 page 30 DNI J1, R519 ,U44 ; Remove SERVO Function

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